A Double-Sided LCL-Compensated Network for the Strongly Coupled CPT System With Minimum Plate Voltage Stresses

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Abstract—In the conventional design of a double-sided LCL compensation network for the capacitive power transfer (CPT) system, two external capacitors are connected in parallel with the horizontal capacitive coupler, or a vertical capacitive coupler is required to reduce the resonant inductances. This approach results in a loosely coupled structure. The compensation inductor resonates with the whole coupler, inducing reactive power transferred from the primary to the secondary side, leading to higher voltage stresses on the plates, which inevitably increases the system complexity and susceptibility to air breakdown. This article proposes a double-sided LCL compensation network design method for the CPT system where no parallel-connected capacitors are required, thereby a strongly coupled structure can be obtained with a constant current (CC) output and input zero phase angle (ZPA) characteristics. By keeping the phase angle difference between the voltage vectors across the primary and secondary plates at 90°, no reactive power is transmitted from the primary to the secondary side. Thus, the voltage stresses across the plates can be minimized. A 500 W prototype with a high coupling coefficient of 0.82 is established to verify the proposed system and an efficiency of 90% is achieved.

Index Terms—Capacitive coupler, capacitive power transfer (CPT), LCL compensation topology, minimum voltage stresses, wireless power transfer (WPT).

I. INTRODUCTION

WIRELESS power transfer (WPT) is emerging as an alternative charging technology in various applications such as electrical vehicles [1], [2], [3], [4], [5], consumer electronics [6], unmanned aerial vehicles [7], [8], [9], automated guided vehicles [10], and autonomous underwater vehicles [11], [12]. According to the transmission mediums, WPT can be mainly classified as inductive power transfer (IPT) and capacitive power transfer (CPT) [13]. In IPT, the energy is transferred by the magnetic field [14]. When metal appears in the magnetic field, the eddy current loss in the metal will cause temperatures to rise, resulting in safety hazards [15], [16]. The CPT system can be presented as a substitute because it transfers energy through the electric field without eddy current issues, which makes CPT technology much safer when metal objects are surrounding. Besides, the CPT system exhibits lower cost and weight because it is made up of copper plates or aluminum plates rather than the Litz wires in the IPT system, which has had a recent wide scope of research [17], [18].

Like in IPT, compensation circuits such as LCLC-LCLC [19], LC-RC [20], LCL-LCL [21], LCL-L [22], and CL-CL [23] are essential to improve the CPT system’s performance. The coupler structure in the CPT system is classified as the horizontal structure and the vertical structure as shown in Fig. 1. The equivalent circuit model and the simplified equivalent Pi model of the coupling capacitors are shown in Fig. 2 [21], [24]. $C_{ij}$ ($i, j = 1, 2, 3, 4; i \neq j$) is the coupling capacitor between $P_i$ and $P_j$. $C_{M}$ and $C_1$ ($C_2$) are the mutual capacitance and the self-capacitance, respectively. The coupling coefficient $k_c$ can be derived as $k_c = C_{M}/C_1 = (C_{13} - C_{14})/(2C_{12} + C_{13} + C_{14})$ because of the symmetrical coupler structure. $C_{13}$ ($C_{24}$) is much larger than $C_{12}$ ($C_{34}$) and $C_{14}$ ($C_{23}$) because the facing area is much larger, thereby the coupling coefficient in a CPT system is essentially high. In [19], a double-sided LCLC-compensated topology with a horizontal coupler structure was proposed. Usually, the self-capacitance in the horizontal coupler structure is only several tens of picofarads. Therefore, two additional capacitors have to be connected in parallel with the coupler to reduce the compensation inductance. However, external capacitors will increase system complexity. To reduce the total number of compensation components, Lu et al. [20] proposed a double-sided LC-compensation circuit topology with a horizontal coupler structure, which includes two external capacitors in parallel with the coupler and two compensation inductors. However, the control degree of freedom is limited.

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because the output power of the system is only related to the
mutual capacitance. Zhang et al. [21] and Vu et al. [22] proposed
a double-sided LCL-compensated topology and an LCL–L
compensation topology, respectively with a vertical coupler
structure. Two plates are placed vertically and close-set on
the primary and secondary sides, respectively to increase the
self-capacitances of the coupler so that no external capacitors
are required. However, since the two plates on the primary
and secondary sides are very close in vertical structure, the
air between them may be prone to breakdown due to the
high electric field. In the above CPT systems, the equivalent
coupling exhibits a low coupling coefficient $k_e$ because the
external capacitors in the horizontal capacitive coupler or
the large self-capacitors in the vertical capacitive coupler
make $C_{13}$ ($C_{23}$) increase, which leads to a loosely coupled
capacitive coupler. Thus, the coupling coefficient in a CPT
system is related to not only plate clearance but also the
external parallel-connected capacitances. It should be noted
that this characteristic is different from the IPT system where
the low coupling coefficient is because of the long distance
between couplers [16].

In the design method shown above, the compensation
inductor resonates with the whole coupler rather than the
self-capacitor, inducing a nonresistive secondary impedance.
Thus, reactive power is transferred from the primary side to
the secondary side, which leads to higher voltage stresses
on the plates. In this case, a strong electric field emission
appears, and the possibility of dielectric breakdown increases.
Moreover, the compensation capacitor’s voltage rating must
be increased, which also increases costs. Thus, Mai et al.
[23] proposed a component voltage stress optimization method
for the double-sided CL-compensated system by reallocating
the voltage stress on the circuit components. Although no
external capacitors are in parallel with the coupler, the com-
ponent voltage optimization design procedure relies on the
initial value, and complicated mathematical calculations are
needed. Lian and Qu [25] and Lian et al. [26] proposed the
parameter design method under the premise of specific coupler
voltage ratings for the double-sided LC-compensated system
and the double-sided LCL-compensated system, respectively.
However, the phase angle difference between the primary-side
and the secondary-side plate voltages is not $90^\circ$, so the
voltage across the coupler is still not at the minimum value.

In this article, a double-sided LCL compensation network
design method for the strongly coupled horizontal capacitive
coupler is proposed. The derived compensation network struc-
ture aligns with that presented in [19] and [21], which are
considered the benchmark for comparison with the proposed
approach. It is noteworthy that [19] and [21] share the same
compensation network design method but employ different
capacitive couplers. Hence, this article collectively refers to
them as the conventional double-sided LCL compensation
network design method. The contributions of this article are
summarized as follows.

1) The proposed design method eliminates two additional
external capacitors in parallel with the coupler, the
compensation circuit is simplified, and the risk of air
breakdown is mitigated.
2) Reactive power transferred between the primary and
secondary sides is eliminated with the proposed compen-
sation network design method. Consequently, the plate
voltage stress can also be minimized.
3) In a strongly coupled scenario, the proposed design
methodology yields significantly smaller compensation
inductances, thereby the system volume is reduced.
Thus, the proposed compensation method is more suit-
able for a strongly coupled CPT system.

The remainder of this article is as follows. Section II
elaborates on the weakness of the conventional design
method for the double-sided LCL-compensated CPT system.
Section III proposes a design method for the double-sided
LCL-compensated CPT system and gives an analysis of volt-
age stresses and system efficiency. Experiment and simulation
results are provided in Section IV to validate the presented
system design method.

II. ANALYSIS OF REACTIVE POWER GENERATION

A. System Description and Reactive Power Analysis

Fig. 3(a) shows the circuit structure of the double-sided
LCL-compensated CPT system. $V_{dc}$ is the dc source. $S_1,$
$S_2,$ $S_3,$ and $S_4$ are four metal oxide semiconductor field
effect transistors (MOSFETs), which form the high-frequency
inverter. $V_{ab}$ is the inverter output voltage. $L_1, C_{11},$ and
$L_1$ form the primary LCL resonate circuit. $L_{f1}, C_{f1},$ and
$L_2$ form the secondary LCL resonant circuit. A full-bridge
rectifier formed by four diodes $D_1, D_2, D_3,$ and $D_4,$ and
a filter capacitor $C_f$ is adopted before a real load $R_o$ at
the receiving side to transform the ac power to a dc source. It
is noteworthy that there is no requirement for external capacitors
to be paralleled with the horizontal coupler. To simplify
the following analysis, the full-bridge rectifier with a real load is
regarded as resistive and can be modeled as a load resistance
$R_L$ [27], and the equivalent behavior-source model is shown in
Fig. 3(b). It should be noted that $C_1$ and $C_2$ only represent the
internal self-capacitances when the proposed design method is
employed. The induced current sources \( I_{M1} \) and \( I_{M2} \) can be expressed as
\[
I_{M1} = -j\omega_0 C M V_{C2}, \quad I_{M2} = j\omega_0 C M V_{C1}
\] (1)
where \( \omega_0 \) is the resonant angular frequency and \( \omega_0 = 2\pi f_0 \). \( f_0 \) is the resonant frequency. \( V_{C1} \) and \( V_{C2} \) are the voltage vectors across the primary plates and the secondary plates, respectively.

The apparent power \( S \) transferred from the primary side to the secondary side is a combination of active power \( P \) and reactive power \( Q \), which can be expressed as
\[
S = P + jQ = V_{C1} \cdot (-j\omega_0 C M V_{C2})^* \tag{2}
\]
where "*" is the conjugate of the corresponding variable. It is noteworthy that the reactive power is zero and the transferred active power reaches the maximum value only when the phase angle difference between \( V_{C1} \) and \( V_{C2} \) is 90°.

In order to discover the condition when the 90° phase angle difference between \( V_{C1} \) and \( V_{C2} \) can be achieved, the secondary side impedance \( Z_{sec} \) in the CPT system of Fig. 3 can be calculated as
\[
Z_{sec} = V_{C2}/I_{M2} = V_{C2}/\left(j \frac{1}{Z_{CM}} V_{C1}\right). \tag{3}
\]

It can be observed from (3) that when the secondary side impedance is resistive, the phase angle difference between \( V_{C1} \) and \( V_{C2} \) is 90°. In this case, no reactive power is transferred from the primary to the secondary side. The product of the primary-side and secondary-side plate voltages can be minimized given the specified active power demand.

**B. Conventional Double-Sided LCL Compensation Network Design Method**

The equivalent behavior-source model of the derived double-sided LCL compensation network employing the conventional design method for the CPT system is the same as in Fig. 3(b) [19], [21]. The resonance conditions derived from the proposed design method differ from those obtained through the conventional design method, in which the compensation inductor resonates with the whole coupler. Furthermore, in the conventional design method, in order to reduce the compensation inductance, two external capacitors have to be connected in parallel to the horizontal capacitive coupler. A critical distinction to note is that \( C1 \) and \( C2 \) incorporate not only self-capacitance but also external capacitance. Alternatively, two plates need to be very close to form a vertical capacitive, thereby increasing the self-capacitances. The resonant conditions are expressed as [19], [21]
\[
\omega^2_0 = \frac{1}{L_1 C_{f1}} + \frac{1}{L_1(1-k^2_c)C_{1}} = \frac{1}{L_2 C_{f2}} + \frac{1}{L_2(1-k^2_c)C_{2}} \tag{4}
\]

The phase angle difference \( \theta_{diff} \) between \( V_{C1} \) and \( V_{C2} \) can be derived as [19], [21]
\[
\theta_{diff} = \arctan \left( \frac{\omega_0 C_{f2} \cdot V_2^2}{C_2(1-k^2_c) P_L} \right) - \arctan \left( \frac{\omega_0 C_{f1}^2 \cdot k^2_c \cdot V_1^2}{C_1(1-k^2_c) P_L} \right) \tag{5}
\]
where \( V_2 \) is the load voltage and \( P_L \) is the output power. The following analysis is taken from the experimental parameters as shown in Section IV, in which \( V_{dc} = 90 \text{ V} \), \( P_L = 500 \text{ W} \), \( C_M = 37.86 \text{ pF} \). According to Fig. 4(a), \( \theta_{diff} \) decreases with the increasing coupling coefficient, which indicates that more reactive power is transferred with a higher coupling coefficient. According to Fig. 4(b), the product of \( V_{C1} \) and \( V_{C2} \) increases with the growing reactive power under the premise of fixed active power. Moreover, the product of \( V_{C1} \) and \( V_{C2} \) increases with increasing coupling coefficient. Thus, if the same amount of active power is required, \( V_{C1} \) or \( V_{C2} \) will increase when more reactive power flows between the primary and secondary sides. This is owing to the fact that the compensation inductor resonates with the whole capacitive coupler, leading to the nonresistive equivalent impedance in the secondary side as indicated in (3).

**III. PROPOSED DOUBLE-SIDED LCL COMPENSATION NETWORK DESIGN METHOD**

Due to the bandpass characteristic of the resonant CPT system, the fundamental harmonics approximation (FHA) method

![Fig. 3. Double-sided LCL-compensated CPT system with a strongly coupled horizontal capacitive coupler. (a) Circuit structure. (b) Equivalent behavior-source model.](image-url)
can be used to analyze the circuit when higher-order harmonics are neglected [21]. Furthermore, all resonate components are assumed to be ideal with no parasitic resistances. In order to eliminate the reactive power transmission in the CPT system, it is imperative to ensure that the phase angle difference between \( V_{C1} \) and \( V_{C2} \) is 90°, which requires the redesign of the compensation circuits.

### A. Derivation of the Compensation Topology

Usually, the L-section matching network [28], [29] or the gyrator model [30] can be used to design the WPT system. Compared to the gyrator model, the L-section matching network with only two components contributes to the simplification of the design process. Thus, this article adopts the L-section matching network to design the system. The schematic of the proposed double-sided LCL-compensated CPT system is shown in Fig. 5, which contains six blocks. Blocks 1, 3, and 5 are voltage-fed reversed L-section matching networks. Block 2 is the current-fed normal L-section matching network. The abovementioned four blocks comprise an inductor reactance and a capacitor reactance of equal value. Block 4 is a capacitor reactance. Block 6 is an inductor reactance and a capacitor reactance of equal value.

The secondary side impedance \( Z_2 \) is 90°. On the secondary side, the fundamental component of inverter output voltage \( V_1 \) is converted to a CC output through Block 1, and then to a CV output \( V_a \) through Block 2, and finally to a CC output \( I_{M1} \) through Block 3. According to (1), \( V_{C2} \) is only relevant to \( I_{M1} \), so \( V_{C2} \) is a CV and can be calculated as

\[
V_{C2} = I_{M1} \cdot \frac{Z_{CM}}{j} = \frac{V_a}{jZ_5} - \frac{Z_{CM}}{j} = \frac{I_a \cdot jZ_2}{jZ_5} \cdot \frac{Z_{CM}}{-j} = \frac{V_1}{jZ_4} - \frac{jZ_2}{jZ_5} \cdot \frac{Z_{CM}Z_2}{Z_1 \cdot Z_3} \cdot V_1
\]

(6)

where \( Z_{CM} = 1/(\omega_0 C_M) \). On the secondary side, \( V_{C2} \) is converted to a CC output \( I_{RL} \) through Block 5, which can be calculated as

\[
I_{RL} = V_{C2}/jZ_5 = Z_{CM}Z_2V_{C1}/(jZ_1Z_3Z_5).
\]

(7)

In Fig. 5, after the coupler is determined with respect to the requirements in the specific application, \( Z_3 \) and \( Z_4 \) are known, which can be expressed as

\[
Z_3 = 1/(\omega_0 C_1), \quad Z_4 = 1/(\omega_0 C_2).
\]

(8)

The secondary side impedance \( Z_{sec} \) can be derived as

\[
Z_{sec} = 1 \sqrt{\frac{R_l}{Z_5^2} + j \left( \frac{1}{Z_4} - \frac{1}{Z_5} + \frac{Z_0}{Z_5^2} \right)}.
\]

(9)

According to (3), \( Z_{sec} \) should be purely resistive to ensure that the phase angle difference between \( V_{C1} \) and \( V_{C2} \) is 90°.

so the following condition should be met:

\[
Z_6 = Z_5(Z_4 - Z_3)/Z_4.
\]

(10)

Considering \( Z_4, Z_5, \) and \( Z_6 \) in (10) are positive, the secondary compensation network is an LCL-compensated circuit as shown in Fig. 5(b), where \( jZ_5, (-jZ_3), \) and \( jZ_6 \) are equivalent to an inductor \( L_2 \), a capacitor \( C_{f2} \), and an inductor \( L_{f2} \), respectively. Furthermore, since the impedance \( Z_4 \) of the self-capacitance in the horizontal coupler is usually large, it can be obtained that \( Z_4 > Z_5 \), which indicates a smaller \( L_2 \) of the secondary compensation circuit.

The secondary side impedance \( Z_{sec} \) seen from the primary side is defined as the reflected impedance \( Z_r \), which can be derived as

\[
Z_r = V_{C1}/I_{M1} = 1/[((\omega_0 C_M)^2 Z_{sec})].
\]

(11)

The primary side impedance \( Z_{in} \) can be calculated as

\[
Z_{in} = 1/[Z_5^2 + j \left( Z_5/Z_2 - 1/Z_1 - Z_5^2/Z_1^2 Z_3 \right)].
\]

(12)

Under the premise that the secondary side impedance is resistive, for the sake of realizing input zero phase angle (ZPA), the following equation should be met to obtain a resistive \( Z_{in} \):

\[
Z_1 = Z_2(Z_3 - Z_2)/Z_3.
\]

(13)

Considering \( Z_1, Z_2, \) and \( Z_3 \) in (13) are positive, it can be obtained that \( Z_3 > Z_2 > Z_1 \), \( jZ_4 \) is equivalent to an inductor \( L_{f1} \). The parallel circuit of \( (-jZ_1) \) and \( jZ_2 \) is equivalent to a capacitor \( C_{f1} \). The series circuit of \( (-jZ_3) \) and \( jZ_3 \) is equivalent to an inductor \( L_1 \). Thus, the primary compensation network is also an LCL-compensated circuit as shown in Fig. 5(a). Moreover, \( Z_3 - Z_2 \) is smaller than \( Z_3 \), so the equivalent inductance \( L_1 \) is not too large, which indicates a smaller inductor of the primary compensation circuit.

It can be obtained from (9)–(13) that the primary side impedance is inversely proportional to the load resistance,
which indicates that the removal of the pick-up does not result in the generation of excessive over-currents and over-voltages. Thus, the proposed system is beneficial to be used in applications where the secondary side moves in and moves out.

B. System Parameter Design

Since \( R_L \) is a purely resistive load, \( I_{RL} \) is in phase with the load voltage \( V_2 \), and the output power \( P_L \) can be derived as

\[
P_L = I_{RL}V_2 = Z_{CM}Z_2V_1V_2/Z_1Z_3Z_5. \tag{14}
\]

According to the power balance, the following equation can be obtained:

\[
V_2 \cdot I_{RL} = V_{C2} \cdot I_{M2}. \tag{15}
\]

Substituting (1) and (7)–(15), \( V_{C1} \) can be derived as

\[
V_{C1} = Z_{CM}V_2/Z_5. \tag{16}
\]

When the output power \( P_L \) is specified, in order to minimize the voltages across the primary side and the secondary side at the same time, \( V_{C1} \) should be equivalent to \( V_{C2} \). Thus, the following equation should be satisfied:

\[
V_1/V_2 = Z_1Z_3/(Z_2Z_5). \tag{17}
\]

Therefore, under the premise that \( V_1, V_2, P_L, \) and the capacitive coupler are specified, substituting (17) into (14), \( Z_5 \) can be calculated as

\[
Z_5 = \sqrt{Z_{CM}V_2^2/P_L}. \tag{18}
\]

\( Z_6 \) can be derived from (10) and (18), which can be expressed as

\[
Z_6 = \sqrt{Z_{CM}V_2^2/P_L} - Z_{CM}V_2^2/(Z_4P_L). \tag{19}
\]

According to (13), (17) and (18), \( Z_2 \) can be calculated as

\[
Z_2 = Z_3 - \sqrt{Z_{CM}V_2^2/P_L}. \tag{20}
\]

\( Z_1 \) can be derived from (13) and (20), which is expressed as

\[
Z_1 = \sqrt{Z_{CM}V_2^2/P_L} - Z_{CM}V_2^2/(Z_3P_L). \tag{21}
\]

Based on (8), (18)–(21), \( Z_1-Z_6 \) are listed in Table I. The compensation inductances and capacitances are calculated as (22). In the case of \( V_1 = V_2 \) and \( Z_3 = Z_4 \), \( L_{f1} = L_{f2}, C_{f1} = C_{f2}, \) and \( L_1 = L_2 \) can be derived. The flowchart of the proposed parameter design for the double-sided LCL-compensated CPT system is shown in Fig. 6.

\[
\begin{align*}
L_{f1} &= \frac{Z_1}{\omega_0} = \frac{1}{\omega_0} \left( \sqrt{\frac{Z_{CM}V_1^2}{P_L} - \frac{Z_{CM}V_2^2}{Z_3P_L}} \right) \\
L_{f2} &= \frac{Z_6}{\omega_0} = \frac{1}{\omega_0} \left( \sqrt{\frac{Z_{CM}V_2^2}{P_L} - \frac{Z_{CM}V_2^2}{Z_4P_L}} \right) \\
C_{f1} &= \frac{Z_2 - Z_1}{Z_1Z_2} = \frac{1}{\omega_0} \sqrt{\frac{P_L}{Z_{CM}V_1^2}} \\
C_{f2} &= \frac{1}{\omega_0Z_5} = \frac{1}{\omega_0} \sqrt{\frac{P_L}{Z_{CM}V_2^2}} \\
L_1 &= \frac{Z_3 - Z_2}{\omega_0} = \frac{1}{\omega_0} \sqrt{\frac{Z_{CM}V_2^2}{P_L}} \\
L_2 &= \frac{Z_5}{\omega_0} = \frac{1}{\omega_0} \sqrt{\frac{Z_{CM}V_2^2}{P_L}}.
\end{align*}
\]

It can be seen from (22) that the system with the proposed design method achieves power enhancement by solely modifying the source voltage and load voltage, without the
need to change any other parameters. By simplifying (22), the resonance condition with the proposed design method can be derived as
\[ \omega_0^2 = \frac{C_1}{(L_1 - L_f)C_f^1} = \frac{C_2}{(L_2 - L_f)C_f^2} = \frac{1}{L_1 C_{f1}} = \frac{1}{L_2 C_{f2}}. \] (23)

Based on (14), (22), and (23), the load-independent CC current output is given by
\[ I_{RL} = \frac{\omega_0 C_{f1} C_{f2} V_1}{C_M}. \] (24)

The input impedance \( Z_{in} \) can be derived by the power balance and is expressed as
\[ Z_{in} = \frac{V_1^2}{I_{RL} R_L} = \frac{C_M^2}{\omega_0^2 C_{f1} C_{f2} R_L}. \] (25)

which indicates that a load-independent CC output and input ZPA are realized.

Fig. 7 gives the parameter comparison between the proposed and the conventional double-sided LCL compensation network design method [19], [21]. It can be observed that in the case of a high coupling coefficient, inductances \( L_1(L_2) \) and \( L_f(L_f) \) with the proposed design method are smaller, while capacitances \( C_f(L_f) \) are slightly larger. It is worth noting that inductances \( L_1(L_2) \) are extremely large with the conventional LCL-compensated network design method, which is not feasible in a practical system. Thus, the conventional double-sided LCL-compensated network design method is not suitable for the strongly coupled system. Besides, it should be noted that the compensation inductances \( L_f(L_f) \) is less than 0 on the condition that \( k_c < 0.085 \) in the proposed system. This is because in this case, \( Z_3 \) decreases and \( Z_2 \) and \( Z_1 \) are less than 0, which is contrary to the premise that all impedances are positive. Thus, the proposed design method is more suitable for the strongly-coupled CPT system.

C. Analysis of the Voltage Stresses and Current Stresses

The voltages across \( L_{f1}, L_{f2}, C_{f1}, C_{f2}, L_1, \) and \( L_2 \) are defined as \( V_{L_{f1}}, V_{L_{f2}}, V_{C_{f1}}, V_{C_{f2}}, V_{L_1}, \) and \( V_{L_2} \), respectively. The voltage stresses in the double-sided LCL-compensated CPT system employing the proposed compensation network design method are listed in Table II. The currents flowing through \( L_{f1}, L_{f2}, C_{f1}, C_{f2}, L_1, L_2, C_1, \) and \( C_2 \) are defined as \( I_{L_{f1}}, I_{L_{f2}}, I_{C_{f1}}, I_{C_{f2}}, I_{L_1}, I_{L_2}, I_{C_1}, \) and \( I_{C_2} \), respectively, and can be obtained by dividing the voltage stress across the compensation circuit components by the impedance. The voltage and current stresses in the double-sided LCL-compensated system employing the conventional compensation network design method can be obtained from [21] in which the voltage stresses of all resonated components have been listed. Fig. 8 illustrates the voltage stress comparison between the proposed and the conventional compensated topology design method. It can be observed that the voltage stresses of the LCL-LCL CPT system employing the conventional design method increase rapidly with the increase of \( k_c \), but with the proposed design method, the voltage stresses gradually stabilize. Additionally, it should be noted that the voltages across \( L_{f1} \) and \( C_{f1} \) with the proposed design method are higher than those of the conventional design method at low coupling regions. The reason is as follows. The voltages across \( L_{f1} \) and \( C_{f1} \) employing the conventional design method are defined as \( V_{L_{f1,con}} \) and \( V_{C_{f1,con}} \), respectively, which can be expressed as [21]

\[
\begin{align*}
L_f,1,con \quad & \quad V_{L_{f1,con}} = \frac{C_M C_{f2} V_2}{1 - k_c^2} \quad \text{and} \quad V_{C_{f1,con}} = V_1 + V_{L_{f1,con}}.
\end{align*}
\] (26)

According to Tables I and II, the voltage across \( L_{f1} \) and \( C_{f1} \) with the proposed design method can be calculated as
\[
\begin{align*}
L_f,1 \quad & \quad V_{L_{f1}} = -\frac{Z_2}{k_c Z_5} V_2 = -\frac{k_c \sqrt{Z_{CM} P_L}}{V_{2k_c}} V_2 \quad \text{and} \quad V_{C_{f1}} = V_1 + V_{L_{f1}}.
\end{align*}
\] (27)

It can be observed from (26) and (27) that \( V_{L_{f1,con}} \) and \( V_{C_{f1,con}} \) are relevant to \( k_c^2 \), \( V_{L_{f1}} \) and \( V_{C_{f1}} \) are relevant to \( k_c \). Thus, at low coupling regions, \( V_{L_{f1,con}} \) and \( V_{C_{f1,con}} \) are larger than \( V_{L_{f1}} \) and \( V_{C_{f1}} \), respectively. It should be noted that the plate voltage stresses are much lower with the proposed design method compared to the conventional design method, especially at regimes of high coupling coefficients. Fig. 9 illustrates the current stress comparison between the proposed and the conventional compensated topology design methods. In systems employing conventional design methods, the currents flowing through the compensation capacitors are higher, especially under the circumstance of high coupling coefficients. Although the currents flowing through the compensation inductors with the proposed method increase with the coupling coefficient, the inductance with the proposed design method is much lower than those in the conventional design method, as shown in Fig. 7. Therefore, the efficiency with the proposed design method is higher in areas of high coupling. Based on the above analysis, the proposed design

![Fig. 7](image_url)

Parameter comparison between the proposed and the conventional compensated topology with different coupling coefficients.
methodology is better suited to an application with a high coupling coefficient.

D. Analysis of the System Efficiency

The system efficiency can be determined using the methodology outlined in [31], which involves listing the node voltage equations for the equivalent circuit to calculate the currents flowing through the compensation circuit components and obtaining efficiency by the ratio of output power to input power. The result reveals that the system efficiency is correlated with both the coupling coefficient and the quality factor. Usually, the quality factors of all compensation components are different. To simplify the efficiency analysis, all quality factors are assumed identical as $Q$. Fig. 10 shows the maximum efficiency comparison between the proposed and the conventional design method versus different coupling coefficients with different quality factors. It can be seen that a higher maximum system efficiency can be obtained with a higher quality factor with both the proposed and conventional design methods. The maximum achievable efficiency declines faster employing the conventional design method under the premise of a high coupling coefficient compared with that in the proposed design method. Besides, with a high coupling coefficient, the inductance $L_1$ ($L_2$) in the double-sided LCL-compensated CPT system employing the conventional design method obtained from [19] and [21] will reach the mH level, which is extremely large and not feasible in a practical system. Thus, the operation region of the double-sided LCL-compensated CPT system with the conventional design method is usually in range A, while the double-sided LCL-compensated CPT system with the proposed design method works in region B, which manifests that the proposed design method can have a higher efficiency. This characteristic also indicates that the proposed design method is beneficial to be applied to the high coupling coefficient scenario.

IV. SYSTEM VERIFICATION

A. Experiment Prototype

A 500 W experiment prototype has been developed as shown in Fig. 11. An inverter consisting of four SiC MOSFETs (C2M0080120D) is used to generate the high-frequency ac power. The dc voltage of the inverter $V_{dc}$ is 90V. The digital controller (TMS320F28335) is employed to generate pulsedwidth modulation signals and the switching frequency is 1 MHz. On the secondary side, a rectifier consisting of four SiC diodes transforms the ac to dc. The coupler is constituted by four aluminum plates with the dimensions of $610 \times 610 \times 2$ mm. The plate separation distance is 300 mm. The air-gap is 50 mm. In this case, the measured mutual capacitance $C_M$ is

Fig. 8. Voltage stress comparison between the proposed design method and the conventional design method for the double-sided LCL-compensated CPT system.

Fig. 9. Current stress comparison between the proposed and the conventional design method for the double-sided LCL-compensated CPT system.

Fig. 10. Maximum achievable efficiency comparison between the proposed design method and the conventional design method versus different coupling coefficients with different quality factors.

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TABLE III
SYSTEM SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_o$</td>
<td>90V</td>
<td>$f$</td>
<td>1MHz</td>
</tr>
<tr>
<td>Plate size</td>
<td>610mm×610mm×2mm</td>
<td>Separation distance</td>
<td>300mm</td>
</tr>
<tr>
<td>Air gap</td>
<td>50mm</td>
<td>$k_c$</td>
<td>0.82</td>
</tr>
<tr>
<td>$C_1$</td>
<td>37.86pF</td>
<td>$C_{D(C)}$</td>
<td>46.34pF</td>
</tr>
<tr>
<td>$L_f$</td>
<td>34.82μH</td>
<td>$L_{ZC}$</td>
<td>34.32μH</td>
</tr>
<tr>
<td>$C_{f1}$</td>
<td>677.68pF</td>
<td>$C_{f2}$</td>
<td>677.68pF</td>
</tr>
<tr>
<td>$L_{1}$</td>
<td>37.38μH</td>
<td>$L_{2}$</td>
<td>37.38μH</td>
</tr>
</tbody>
</table>

Fig. 11. Experiment prototype.

about 37.86 pF, the measured self-capacitances $C_1$ and $C_2$ are about 46.34 pF, and the coupling coefficient $k_c$ is about 0.82. The compensation inductors are made by 1200-strand Litz wires on a hollow plastic tube so that the conduction losses caused by the skin effect can be reduced. The compensation capacitors are formed by connecting multiple high-frequency film capacitors from KEMET in series and parallel to increase the withstand voltage and reduce the internal resistance. The system parameters are listed in Table III, which are obtained by using the process shown in Section III. It should be noted that the premise of obtaining the parameters is to ensure that the phase angle difference between $V_{C1}$ and $V_{C2}$ is 90°, and $V_{C1} = V_{C2}$ with a CC output and input ZPA.

In practical applications, the strict input ZPA will increase the switching noises of the inverter, which induces system efficiency decrease and electromagnetic interference increase, especially for high-frequency applications [32]. The way to solve it is to make the input current $I_{L1}$ lag inverter output voltage $V_{in}$ to facilitate zero-voltage switching (ZVS) [33]. According to (7), the output current $I_{RL}$ is related to $Z_{CM}$, $Z_1$, $Z_2$, $Z_3$, $Z_5$, and $V_1$. In order not to affect the CC output characteristic, $Z_6$ can be adjusted to achieve ZVS. Thus, $L_{f2}$ is slightly smaller than $L_{f1}$ for the system to achieve ZVS.

B. Experiment Results

Fig. 12 illustrates experimental waveforms for load current $I_o$, inverter output voltage $V_{ab}$, inverter output current $I_{L1}$, rectifier input voltage $V_{cd}$, and rectifier input current $I_{L2}$ under conditions of half load, 75% load, and full load conditions. The load currents are around 5.27, 5.16, and 5.06 A, respectively. It shows that load output currents are nearly constant with different loads, which verifies that a CC output is achieved. The slight change in output current is caused by the parasitic resistances of the inductors and couplers. The corresponding system efficiency reaches 86%, 89%, and 90%, respectively. Table IV lists the experimental data. The inverter output voltages and currents are nearly in phase, which shows that the system has achieved the ZVS of MOSFETs. It is worth noting that the increase in the impedance angle with the decrease in load resistance is due to $L_{f2}$ being slightly less than $L_{f1}$ to achieve ZVS. Furthermore, the greater $L_{f2}$ is reduced to achieve ZVS, the greater the variation in input impedance angle.

Fig. 13 shows the output load currents against the normalized load resistance with different input voltages. The current fluctuation ratio $\beta$ is adopted to evaluate the CC output characteristic and is defined by

$$\beta = (I_{max} - I_{min}) / I_{max}.$$  (28)

It can be readily observed that $\beta$ consistently remains below 5% amidst the normalized load resistance within 0.25–1, substantiating the robustness of the CC output. Furthermore, the power and efficiency performance across varied load scenarios with the input dc voltage within 75–90 V as illustrated in Fig. 14. It is worth noting that the system efficiency reaches 90% when the output load power is 500 W with an input voltage of 90 V when the normalized load resistance is 1. The maximum dc–dc efficiency reaching 90.7% is attained under a 75 V dc input voltage and an output power of 173 W. Table V lists the measured output currents and efficiency with different load resistances and power levels.

Fig. 15 illustrates the maximum system efficiency variation with an increasing coupling coefficient. The coupling coefficient can be adjusted by adding different external capacitors parallel to the capacitive coupler. In this case, only the
Fig. 12. Experiment waveforms with different load resistance at $k_c = 0.82$.
(a) Half load. (b) 75% load. (c) Full load.

Fig. 13. Experiment results of output load current $I_o$ against load resistance with different dc sources.

Fig. 14. Experiment results of system efficiency against load power with different dc sources.

Fig. 15. Experiment results of system efficiency against coupling coefficient.

$L_{f2}$ become. The red curve is the calculated ac–ac efficiency, while the red dots represent the measured complete dc–dc system efficiency, including losses from both the inverter and rectifier. At coupling coefficients of 0.15, 0.26, 0.39, 0.53, 0.67, and 0.82, the measured maximum system efficiencies achieved are 91.5%, 90.6%, 91.2%, 89.9%, 90%, and 90.3%, respectively. The experimental data are listed in Table VI. It can be observed that the efficiency of the proposed method does not significantly change with the coupling coefficient and is consistent with the calculated efficiency trend.

The power loss ratio of the proposed design method with $k_c = 0.82$, $V_{dc} = 90$ V, and $P_o = 500$ W is shown in Fig. 16. Only the conduction loss is considered in the inverter because of ZVS [21]. The drain–source on-state resistance of MOSFET and the diode forward voltage of the reverse diode can be obtained from the datasheet. The power loss of the compensation component is caused by the current flowing through its parasitic resistance. The currents flowing through the inverter and compensation components can be calculated by solving Kirchhoff’s current equations, then the power losses of the inverter and the compensation components can be estimated. Subtracting the loss of the inverter and all compensation components from the total loss from the measured efficiency, the loss of the coupler can be acquired [21]. The coupler plates

<table>
<thead>
<tr>
<th>Coupling coefficient</th>
<th>0.15</th>
<th>0.26</th>
<th>0.39</th>
<th>0.53</th>
<th>0.67</th>
<th>0.82</th>
</tr>
</thead>
<tbody>
<tr>
<td>System efficiency</td>
<td>91.5%</td>
<td>90.6%</td>
<td>91.2%</td>
<td>89.9%</td>
<td>90%</td>
<td>90.3%</td>
</tr>
</tbody>
</table>

TABLE VI
MEASURED SYSTEM EFFICIENCY

<table>
<thead>
<tr>
<th>Coupling coefficient</th>
<th>0.15</th>
<th>0.26</th>
<th>0.39</th>
<th>0.53</th>
<th>0.67</th>
<th>0.82</th>
</tr>
</thead>
<tbody>
<tr>
<td>System efficiency</td>
<td>91.5%</td>
<td>90.6%</td>
<td>91.2%</td>
<td>89.9%</td>
<td>90%</td>
<td>90.3%</td>
</tr>
</tbody>
</table>
dissipate 43% of the power loss, which is significantly higher than other components.

Usually, the differential probe is used to measure the plate voltage. However, the proposed CPT system works at a high frequency (1 MHz), which is sensitive to parameter fluctuation. The differential probe contains an active circuit structure, and the intrinsic capacitance of the differential probe will have a large impact on the system because the intrinsic capacitances of differential probes are involved in resonance. In order to verify that the proposed voltage stresses are minimized, two external capacitors are added in parallel with the coupler and then the currents flowing through the external capacitors \( C_{ex1} \) and \( C_{ex2} \) are measured. When two small external capacitors are in parallel connected to the capacitive coupler with a coupling coefficient of 0.74, the currents flowing through the external capacitors are only 0.043 A, which is exceedingly small and challenging to measure accurately using current probes. Additionally, the current flowing through the external capacitor is directly proportional to the external capacitance. Consequently, in order to address this issue, two larger external capacitors, each with a capacitance of 100 pF, are connected in parallel with the coupler, thereby reducing the coupling coefficient \( k_c \) to 0.26. Since the mutual capacitance \( C_M \) is not changed, the compensation inductances \( L_1 \) and \( L_2 \) are the same as that in Table III and only the compensation inductance \( L_{f1} \) and \( L_{f2} \) are reduced to 29.31 \( \mu \)H. Fig. 17 illustrates experimental waveforms for the load current \( I_o \), inverter output voltage \( V_{ab} \), inverter output current \( I_{L f1} \), rectifier input voltage \( V_{cd} \), and the currents flowing through external capacitors \( I_{Cex1} \) and \( I_{Cex2} \) under conditions of half load, 75% load, and full load conditions. The output load currents with the above three different load resistances are nearly constant, which shows that CC outputs are achieved. The phase angle difference between the primary-side plate voltage and the secondary-side plate voltage is around 90\( ^\circ \), which indicates no reactive power is transferred and the plate voltages are minimized. The measured currents flowing through the external capacitors are shown in Table VII. The currents flowing through the secondary-side external capacitor \( I_{Cex2} \) are nearly constant because the voltage \( V_{C2} \) is independent of the load resistance. The currents flowing through the primary-side externally connected capacitor \( I_{Cex1} \) exhibit a direct proportionality to load resistance variation, and the currents flowing through the two externally connected capacitors are nearly equal at full load, with minor variations attributed to parasitic resistances within the system.

### C. Comparison With Existing Works

Recently, voltage stress optimization has been considered a viable approach to mitigate the risks of air breakdown and electromagnetic interference in CPT systems. Lian et al.
[26] has proposed a parameter design method for an LCLC-compensated CPT system, in which three frequencies have been found to realize input ZPA and load-independent CC output under the premise of predesigned voltage stresses. The first frequency \( \omega_0 \) is consistent with the conventional design method in [19] and [21]. The other two frequencies are \( \omega_{1H} \) and \( \omega_{1L} \), which can be expressed as

\[
\omega_{1H} = \omega_1 \sqrt{1 + \alpha}, \quad \omega_{1L} = \omega_1 \sqrt{1 - \alpha}
\]

(29)

where

\[
\alpha = \sqrt{(1 - k_2^2)(C_2/C_{f2})^2 + (C_2/C_{f2})(1 - k_2^2) + k_2^4} / \left[1 + (1 - k_2^2)(C_2/C_{f2})\right]
\]

Applying the design method in [26] with the experimental coupler dimensions, the operating frequency is chosen to be 1 MHz with the predesigned minimum plate voltages of 2060 V for \( \omega_0 \) and \( \omega_{1H} \), and 2050 V for \( \omega_{1L} \). The calculated parameters with the optimized method in [26] are shown in Table VIII, along with a comparison to the parameters of the proposed method as well as the conventional method in [19] and [21]. It should be noted that there is no solution for \( \omega_{1L} \). The compensation inductances are significantly reduced in the proposed method compared to the conventional method in [19] and [21]. Furthermore, unlike the optimization method in [26], no external compensation capacitors parallel to the capacitive coupler are needed, and there is a significant reduction in compensation inductances compared to the optimized parameters operating at \( \omega_{1H} \).

In the experimental setup, the parasitic capacitance of the probes affects circuit resonance, preventing direct measurement of the voltage stress across the plates. Therefore, voltage distribution on the plates is simulated and finite element simulations are employed to demonstrate electric field radiation. Without considering any parasitic resistances, the voltage stresses across the capacitive coupler in the double-sided LCL-compensated CPT system with the proposed and the conventional compensation network design method as well as the parameter design methods from [26] are simulated using LTspice, as shown in Fig. 18. Using the conventional design method, the rms values of the plate voltages are 3250 V, and the phase angle difference between the primary-side plate voltage and the secondary-side plate voltage is 11.46°, indicating that more reactive power is transferred. When the optimized design method in [26] is employed, the plate voltages at resonant frequencies \( \omega_1 \) and \( \omega_{1H} \) are both 1457 V with an increased phase angle difference of 82°, indicating that the plate voltages are not minimized, hence reactive power still exists. It is worth noting that the phase angle difference between the primary-side plate voltage and the secondary-side plate voltage is 90° with the proposed design method. This indicates no reactive power is transferred and the plate voltages are minimized, with rms values of 1450 V, significantly lower than the conventional design method. Based on the voltage stresses depicted in Fig. 18, the radiation of the leakage electric flux with the proposed and conventional design methods as well as the optimized method mentioned in [26] was investigated using Ansys/maxwell, and the results are presented in Fig. 19. In accordance with the IEEE standard [19], which sets the safety limit for electric fields at 1 MHz to be 614 V/m concerning human safety considerations, it is evident that the conventional design method requires a larger safe distance of 674 mm, the optimized design method in [26] requires a safe distance of 427 mm. The results mentioned above are listed in Table IX. This comparative analysis underscores the advantages of the

---

### Table VIII
CALCULATED PARAMETERS WITH DIFFERENT DESIGN METHODS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Method</th>
<th>( \omega_0 ) in [26]</th>
<th>( \omega_{1H} ) in [26]</th>
<th>Proposed method</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{11} )</td>
<td>0pF</td>
<td>505.06pF</td>
<td>582.98pF</td>
<td>0pF</td>
</tr>
<tr>
<td>( C_{22} )</td>
<td>0pF</td>
<td>505.06pF</td>
<td>582.98pF</td>
<td>0pF</td>
</tr>
<tr>
<td>( C_0 )</td>
<td>478.27pF</td>
<td>9.8076pF</td>
<td>9.6944pF</td>
<td>677.68pF</td>
</tr>
<tr>
<td>( L_1 )</td>
<td>1696.69µH</td>
<td>48.738µH</td>
<td>582.46µH</td>
<td>37.78µH</td>
</tr>
<tr>
<td>( L_2 )</td>
<td>1696.69µH</td>
<td>48.730µH</td>
<td>580.46µH</td>
<td>37.78µH</td>
</tr>
<tr>
<td>( L_3 )</td>
<td>52.96µH</td>
<td>2.5587µH</td>
<td>504.47µH</td>
<td>34.82µH</td>
</tr>
<tr>
<td>( L_p )</td>
<td>52.96µH</td>
<td>2.5587µH</td>
<td>504.47µH</td>
<td>34.82µH</td>
</tr>
</tbody>
</table>

---

### Table IX
VOLTAGE STRESS COMPARISON

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Method</th>
<th>( \omega_0 ) in [26]</th>
<th>( \omega_{1H} ) in [26]</th>
<th>Proposed method</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{C1} ), ( V_{C2} )(RMS)</td>
<td>3250V</td>
<td>1457V</td>
<td>1457V</td>
<td>1450</td>
</tr>
<tr>
<td>( \theta )</td>
<td>11.46°</td>
<td>82°</td>
<td>82°</td>
<td>90°</td>
</tr>
<tr>
<td>Safe distance</td>
<td>674mm</td>
<td>432mm</td>
<td>432mm</td>
<td>427mm</td>
</tr>
</tbody>
</table>
proposed design method, as it exhibits fewer compensation components, smaller compensation inductance, significantly lower voltage stresses, and reduced electric field emissions. These characteristics make it a highly promising choice for applications requiring high power levels.

V. CONCLUSION

This article proposes a double-sided LCL compensation network design method for the strongly coupled CPT system. Both ZPA and CC output characteristics can be obtained. No external capacitors are needed, and no reactive power is transferred from the primary side to the secondary side. Therefore, the voltage stress across the coupler plates is minimized. Compared with the conventional double-sided LCL-compensated network design method, the compensation inductances in the proposed design method are greatly reduced especially in the strongly coupled scenario, along with a substantial decrease in the radiation of the leakage electric flux. Experimental results have verified the proposed double-sided LCL compensation network design method and the experimental system can achieve 90% efficiency when 500 W power is delivered.

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REFERENCES


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