# A functional model of silicon carbide JFET and its use in the analysis of switching-transient and impact of gate resistor, miller effect and parasitic inductance

Hua Bai, Sanbo Pan and Chris Mi*

University of Michigan-Dearborn,
4901 Evergreen, Dearborn, MI 48128, USA
E-mail: baihua@umd.umich.edu
E-mail: pansansjtu@hotmail.com
E-mail: chrismi@umich.edu
*Corresponding author

Tim Lin

Aegis Technology, Inc.,
12630 G. Westminster Ave.,
Santa Ana, CA 92706 USA
E-mail: timlin@aegistech.net

**Abstract:** A functional model of silicon carbide (SiC) JFET was developed to study its performance. Based on this model, the gate resistor in the gate drive circuit of SiC JFET is optimised with comprehensive consideration of gate current impact, miller effect, switching speed and voltage spikes. The switch on oscillation caused by parasitic inductance is analysed and methods are proposed to mitigate the oscillation. Experiments on a 300 V prototype validated the proposed model.

**Keywords:** silicon carbide; JFET; inverter; miller effect; switching process; parasitic inductance; power electronics.

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**Biographical notes:** Hua BAI received his BS and PhD in Electrical Engineering from Tsinghua University, Beijing, China in 2002 and 2007, respectively. He is an Assistant Research Scientist in University of Michigan, Dearborn, MI, USA. His research interests include the dynamic processes and transient pulse power phenomena of power electronic devices, especially in the high voltage high power inverter and isolated bidirectional DC-DC converter.

Sanbo Pan received his BEng and MEng in Electrical Engineering from Huazhong University of Science and Technology, Wuhan, China, in 1986 and 1988, respectively. He received his PhD in Electrical Engineering from Shanghai Jiao Tong University, Shanghai, China, in 2007. From 2007 to 2008, he was a Post Doctorial Researcher in University of Michigan, Dearborn, USA. His research interests are SiC power devices, solar inverters and power electronics.

Chris Mi is Associate Professor of Electrical Engineering at the University of Michigan, Dearborn. He received his BSEE and MSEE from Northwestern Polytechnical University, China, and his PhD from University of Toronto, Canada. His research interests are in power electronics, hybrid electric vehicles, electric machines and renewable energy systems. He worked for General Electric Canada Inc. from 2000 to 2001. Chris Mi is the recipient of numerous awards including the Distinguished Teaching Award and Distinguished Research Award from the University of Michigan, National Innovation Award and Government Special Allowance Award from China, and IEEE and SAE Awards. He is a Senior Member of IEEE and has more than 100 publications.

Timothy Lin received his PhD in Engineering from University of California, Irvine, 2000. He is the Technical Director and Co-Founder of Aegis Technology. His primary research areas include nanomaterial and advanced joining technology for a variety of applications (lightweight armours, energy storages, solid oxide fuel cell, Li-ion batteries, thermoelectric cooling and energy harvesting); thermal management and packages for high power, high power density electronics for motor drive, energy storage, laser diode arrays and microwave appliers; and high temperature electronics based on SiC power devices. He is an IEEE Senior Member and has more than 30 technical publications.

## 1 Introduction

A silicon carbide (SiC) semiconductor has a wide bandgap (3.0 eV for 6H-SiC), high saturation velocity ($2 \times 10^7$ cm/s), high thermal conductivity (3.3–4.9 W/cmK), low on-state resistance (1 m$\Omega$/cm$^2$) and high breakdown electric field strength (2.4 MV/cm) (Ozpineci and Tolbert, 2003; Funaki et al., 2007; Yan et al., 2006). Therefore, SiC-based power devices are expected to show superior performance compared to traditional silicon (Si) power switches. Since SiC power devices can operate at higher switching frequencies (Abou-Alfotouh et al., 2006), the size of passive components (inductor and capacitor) can be significantly reduced in SiC-based power electronic converters. The associated heatsink size will also be reduced due to the lower losses compared with a conventional power electronic converter. It is predicted that SiC devices will have significant impact in the next-generation power electronic systems (Inoue and Akagi, 2007).

While SiC MOSFET and SiC IGBT are difficult to fabricate at the present time, SiC JFET is easier to manufacture. Therefore, of all SiC power transistors currently under development (e.g., MOSFETs, JFETs, BJTs, IGBTs), SiC JFETs have the greatest potential for near-term real world applications. With extensive research and development effort underway, it is anticipated that more SiC JFET will be used in power electronic systems.

The biggest barrier of using SiC JFETs is its 'normally on' characteristic (Kelley and Mazzola, 2006). One feasible solution is to use an SiC JFET cascade with a low on-resistance Si MOSFET to form a normally off SiC switch (Round et al., 2005). The control becomes easier, but the additional Si MOSFET will add system cost and generate additional losses. Another solution is to use a negative voltage to turn off the SiC JFET switches (Kelley and Mazzola, 2006).

In the latter case, to study the performance of SiC JFET, a functional model is needed to help the circuit design (the selection of gate drive parameters), testing (transient electrical pressure), prototyping and product development (high temperature operation). Some JFET models have been developed based on existing models of Si-based power devices (Kashyap et al., 2004). However, these models have large deviations from the actual SiC devices in both static and dynamic performance.

This paper established a functional model through the testing of a three-phase two-level SiC inverter. Based on this model, the gate resistor is optimised and the switch on oscillation is analysed. The effect of miller-capacitance during switch on/off transients is also discussed. Experimental results on a 300 V prototype validated the analysis.

## 2 SiC JFET model and experimental verification

Different approaches can be used to develop models of power electronic devices (Kashyap et al., 2004; McNutt et al., 2007). The model of SiC device developed in this paper adopts the method proposed in Kashyap et al. (2004). In this model, a voltage controlled current source is used to simulate the current in the JFET channel as shown in (1). The junction capacitors are expressed in (2) and (5). Since the main concern is the transient process, the on/off state equations are ignored.

$$I_{JFET} = i_0[1+\tanh\{P(V_{gs}-V_{th})\}]\bullet\tanh(\alpha V_{ds})e^{\lambda V_{ds}} \quad \text{if} \quad V_{ds}\geq 0 \tag{1}$$

$$W_{gs} = \sqrt{\frac{2\varepsilon|V_{gs}-V_{th}|}{qN_b}} \tag{2}$$

$$W_{gd} = \sqrt{\frac{2\varepsilon|V_{gd}-V_{th}|}{qN_b}} \tag{3}$$

$$C_{gs} = \frac{f_{csj}A_s\varepsilon}{W_{gs}} \tag{4}$$

$$C_{gd} = \frac{A_g\varepsilon}{W_{gd}} \tag{5}$$

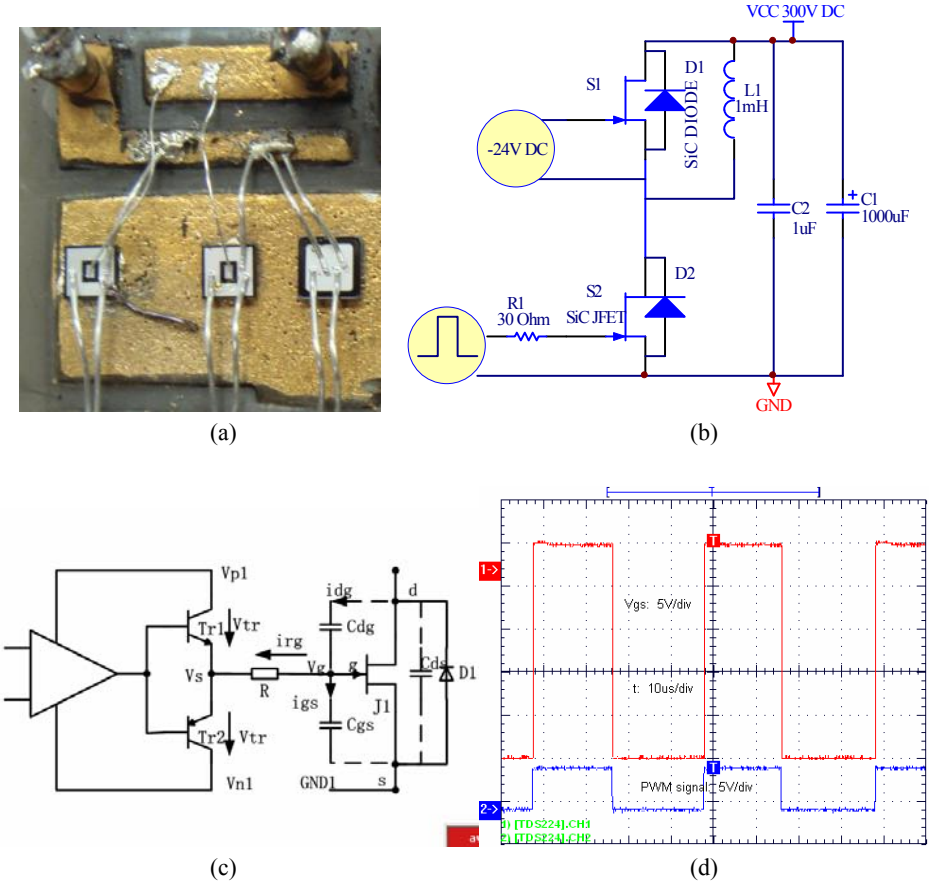
where $V_{gs}$ is the gate voltage, $V_{gd}$ is the voltage across gate to drain, $V_{th}$ is the threshold voltage to turn on/off the *JFET* and $V_{ds}$ is the voltage across drain to source. $W_{gs}$ is the depletion width of gate source area, $W_{gd}$ is the depletion width of gate drain area, $q$ is the fundamental electronic charge, $N_b$ is the base dopant density, $A_g$ and $A_s$ are gate drain and gate source overlap area.

In (1), the first item is for conductivity modulation by gate voltage and the second term is for non-linear relationship between $V_{ds}$ and $I_{ds}$. In order to determine the parameters in (1)–(5), the voltage/current waveforms under specific operational conditions are tested to fit the waveforms with simulated results by adjusting the relevant parameters in the functional model (1)–(5).

The SiC module used for the three-phase inverter is shown in Figure 1(a). Two parallel connected SiC JFETs are on the left side and an SiC freewheel diode is on the

right side. Besides that, a paralleled SiC Skottky diode is used to mitigate the reverse recovery current. Therefore, the diode model here is beyond our concern. Because of the 'normally on' feature, the SiC JFET turns on at zero gate voltage. A negative voltage, usually –24 V to –30 V, is necessary to turn off the SiC JFET. In our design, an optical coupler is used to isolate the upper and lower driver circuit in the same bridge, as shown in Figure 1(b). The totem pole stage amplifies the driver capability followed by the gate resistor as in Figure 1(c). The gating control logic is shown in Figure 1(d). When PWM signal from the digital controller is high, the gating voltage is equal to $V_{CC}$ (0 to 5 V) and the SiC JFET turns on. Otherwise, the gating voltage is equal to $V_{SS}$ (–24 V to –30 V) and the SiC JFET turns off.

**Figure 1** Test platform, (a) tested SiC JFET and diode (b) hardware platform (c) gate drive circuit (d) gate drive waveforms (see online version for colours)



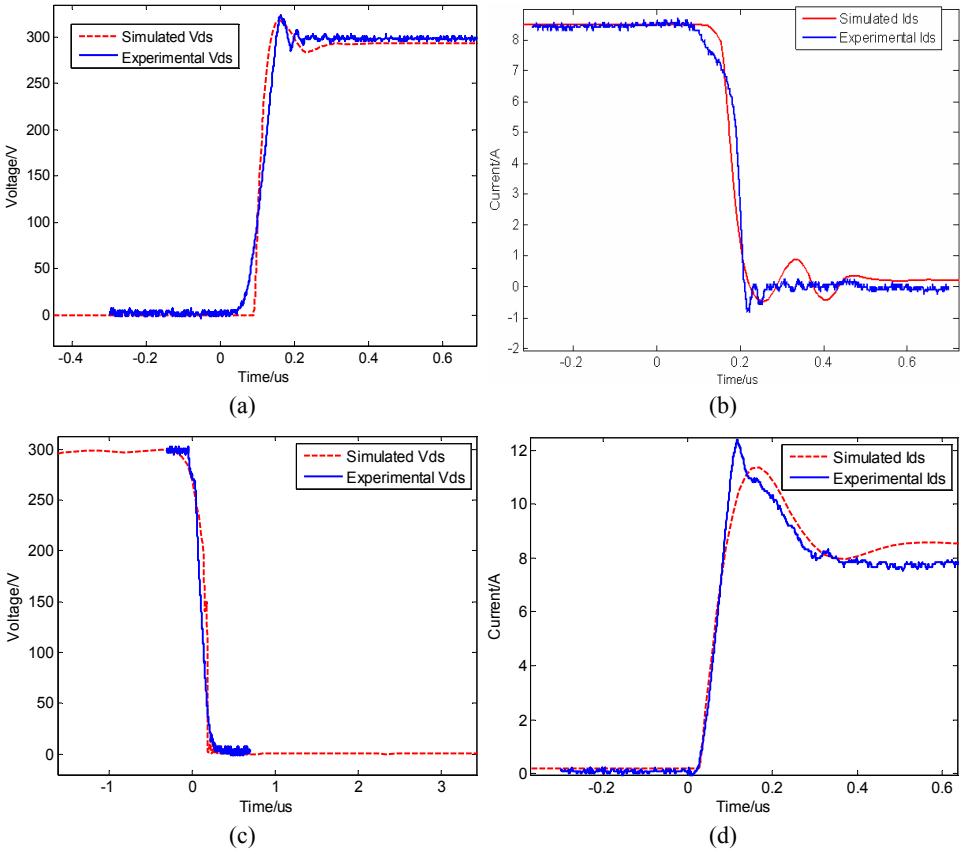

The transient performance of the SiC JFET is simulated based on (1)–(5). The turn on and turn off voltage/current are compared to the experimental results and the relevant parameters are adjusted to match the waveforms. Figure 2 shows the comparison of experimental and simulated switch on/off processes of an SiC JFET at 300 V/8A with a gate drive resistor equal to 1 Ω. The simulated results coincide with experimental waveforms for both turn on and turn off processes.

The parameters listed in (1)–(5) are approached by the experimental waveforms, which are shown in Table 1.

**Table 1** Approached parameters

| *Parameter* | *Value* |
|---|---|
| $\alpha$ | 0.298 ($V^{-1}$) |
| $\lambda$ | 0.03 ($V^{-1}$) |
| $V_{th}$ | –18 (V) |
| $P$ | 1.6 ($V^{-1}$) |

**Figure 2** Comparison of simulated and experimental results, (a) turn off voltage $V_{ds}$ (b) turn off current $I_{ds}$ (c) turn on voltage $V_{ds}$ (d) turn on current $I_{ds}$ (see online version for colours)




## 3 Optimisation of gate drive resistance based on SiC JFET model

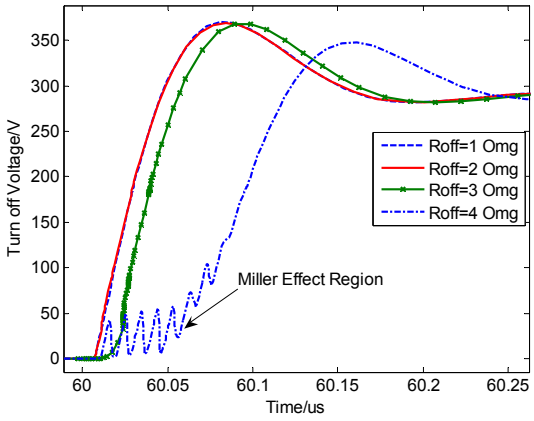
It was observed during the experiment and simulation that the gate resistance is of critical importance in SiC JFET-based inverter design. In Figure 1(c), a smaller $R$ will increase the switching speed, but will also induce a large voltage spike due to stray inductance.

Meanwhile, it has large current impact on the gate during switching process. A larger $R$ will slow the switching process, thereby, increases the switching loss.

If a gate resistance is not appropriately chosen, miller effect (Theodoridis and Mollov, 2008) will emerge. A big difference between gate power supply voltage and the actual $V_{gs}$ will exist. This difference is caused by the following:

1 For a single SiC JFET, there is a charge/discharge current through the drain capacitor $C_{dg}$, thereby, gate miller capacitor $C_{gs}$ during on/off process. For turn off process, the rise of $V_{ds}$ induces a current through $C_{dg}$ as well as $C_{gs}$ and changes the $V_{gs}$. If $R$ is large, the excessive charge continuously accumulated on the gate will slowly discharge to the gate power supply. Therefore, the JFET may be turned on by the miller effect. Figure 3 shows the turn off voltage under different gate resistance. It can be seen that $R = 1\ \Omega$ is the appropriate choice. When $R = 4\ \Omega$, the JFET is turned on/off frequently by the miller effect.

**Figure 3** Turn off voltage under different gate drive resistors (see online version for colours)




2 For an SiC JFET bridge, during the commutating process, the gate voltage of one JFET could be directly influenced by the turn on/off process of another interlocked device. In Figures 4(a)–(b), the upper drive resistor ($R_U$) is kept constant and the gate drive resistor of the lower JFET ($R_L$) varies. In Figure 4(a), $R_L$ is small. The switch on process of the lower JFET increases the voltage across the upper JFET and turns on the upper interlocked device. Therefore, a large current spike appears. If $R_L$ is small enough (i.e., dv/dt is large enough), the increased voltage drop will cause a shoot-through of the bridge. In Figure 4(b), this spike disappears with a larger $R_L$. The switching speed is also slowed due to the increase of $R_L$.

3 With the same drive resistance, the larger the DC-link voltage or dv/dt, the more significant the miller effect. Figures 4(c)–(d) show the ripples of the gate source voltage of the upper JFET (constant –24 V is applied on the gate at all times) when the lower JFET is switched with different DC-link voltage. The larger the DC link voltage, the more severe the miller effect.

Therefore, the gate drive resistor must be optimised. The influence of gate drive resistor on the transient performance of SiC device is shown in Table 2.

**Table 2** Influence of gate resistor on device performance

| | *Switching speed* | $I_{gs}$ | *Miller effect* | *Inductive spikes* |
|---|---|---|---|---|
| Large $R$ | Slow | Small | Large | Small |
| Small $R$ | Large | Large | Small | Large |

**Figure 4** Experiment of miller effect, (a) current with high spike (upper diode) (b) current without high spike (upper diode) (c) drive voltage $V_{DC}$ = 200 V (upper JFET) (d) drive voltage $V_{DC}$ = 400 V (upper JFET) (see online version for colours)

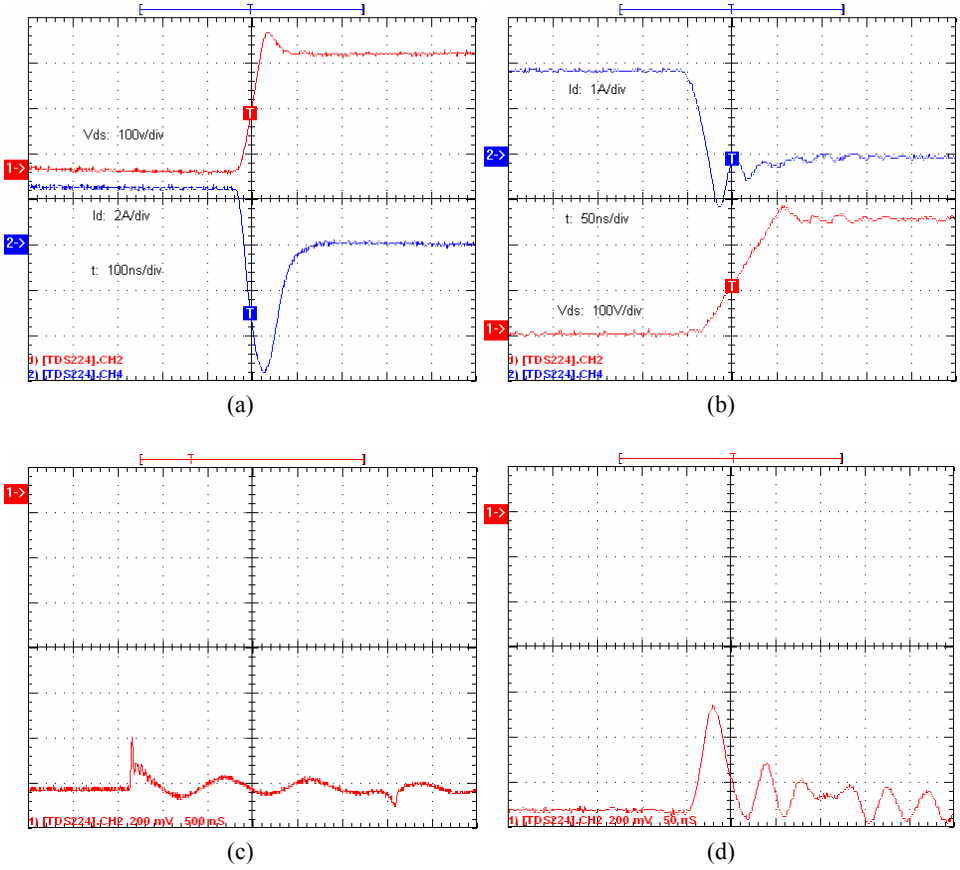
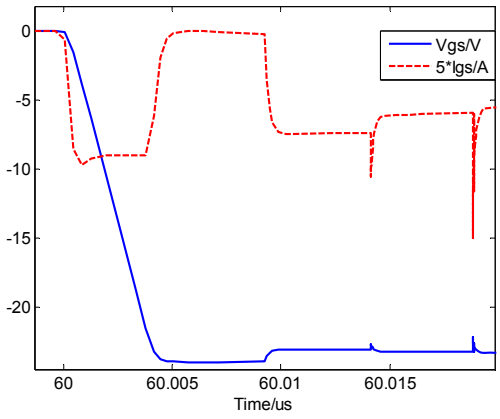
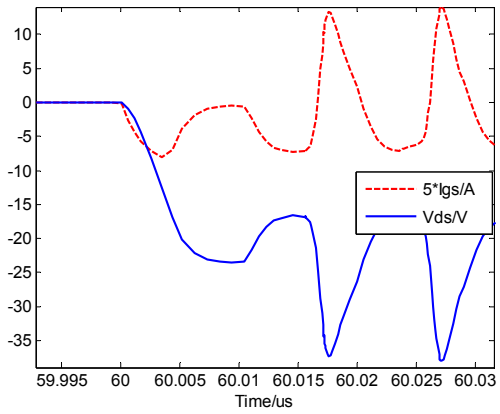



Figure 5 shows the impact of gate current during switching process for different gate drive resistance. Because the time constant of gate drive circuit is small (resistor is in ohms and $C_{dg}/C_{gs}$ is in pF) and the rising/trailing edge of $V_s$ in Figure 1(c) is in nanoseconds. Therefore, the time constant of $V_g$ in Figure 1(c) is actually less than that of $V_s$, which makes the gate switch on/off current not significantly increased when $R$ decreases. However, when $R$ < 1 Ω, a small variation of the gate signal can cause large impact on gate current. This means that the system is susceptible to the variation of gate power supply or any other disturbance in the steady state. When $R$ = 5 Ω, the miller effect appears. In this design, the optimal resistance is 1 Ω.

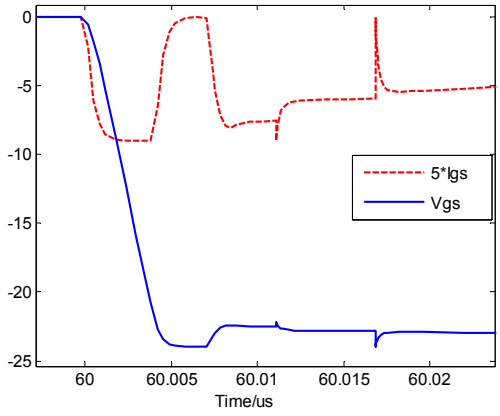
**Figure 5** Simulated gate voltage/current with different gate resistance, (a) $R = 0.5\ \Omega$ (b) $R = 5\ \Omega$ (c) $R = 1\ \Omega$ (see online version for colours)




(a)




(b)




(c)

## 4 Switching transients

In order to measure the current in the test platform, a moderate length of wire has to be added to connect the DC bus and switches. This parasitic inductance of the wire also has impact on the switching performance. In the experiment, there is a high frequency oscillation during the turn on, which is caused by the parasitic inductor, junction capacitor and equivalent turn on resistor of the SiC JFET. The oscillation can be described using a second-order differential equation. Assume $C_D$ is the equivalent junction capacitor of the diode and remains constant, then the expression of the diode voltage ($V_D$) can be derived:

$$\begin{cases} \dfrac{d^2V_D}{dt^2}+\dfrac{R}{L_r}\cdot\dfrac{dV_D}{dt}+\dfrac{1}{L_r\cdot C_D}\cdot V_D=\dfrac{1}{L_r\cdot C_D}(V_{DC}-i_LR_s) \\ V_D(0)=0 \\ C_D\dfrac{dV_D}{dt}(0)=I_{rrm} \end{cases} \tag{6}$$

The expression of diode voltage $V_D$ and diode current ($I_D$) are

$$\begin{cases} V_D(t)=\dfrac{I_{rrm}/C_D-\lambda_2(i_LR_s-V_{DC})}{\lambda_1-\lambda_2}e^{\lambda_1 t}+\dfrac{\lambda_1(i_LR_s-V_{DC})-I_{rrm}/C_D}{\lambda_1-\lambda_2}e^{\lambda_2 t}+(V_{DC}-i_LR_s) \\ I_D(t)=\dfrac{\lambda_1 I_{rrm}/C_D-\lambda_1\lambda_2(i_LR_s-V_{DC})}{\lambda_1-\lambda_2}e^{\lambda_1 t}+\dfrac{\lambda_2\lambda_1(i_LR_s-V_{DC})-\lambda_2 I_{rrm}/C_D}{\lambda_1-\lambda_2}e^{\lambda_2 t} \end{cases} \tag{7}$$

where $\lambda_{1,2}=\dfrac{-\dfrac{R_s}{L_r}\pm\dfrac{2}{\sqrt{L_rC_D}}\sqrt{m^2-1}}{2}$ and the damping efficient $m=\dfrac{R_s}{2}\sqrt{\dfrac{C_D}{L_r}}$.

When $m > 1$, the circuit is over damped, i.e., no oscillation.

When $m = 1$, the circuit is critical damped.

When $m < 1$, the circuit is under damped and the oscillation frequency is $\dfrac{\sqrt{1-m^2}}{2\pi\sqrt{L_rC_D}}$.

There are two ways to eliminate the turn on oscillation. One way is to shorten the wire to reduce stray inductance $L_r$ and achieve larger damping coefficient. Another way is to use an RC snubber circuit or a larger $C_D$. Figure 6 shows the simulation results based on different stray parameters. In real applications, the oscillating frequency/amplitude may vary due to the non-linearity of junction capacitor and switch on characteristics of SiC JFET.

**Figure 6** Turn on current oscillation of JFET with different stray inductance (see online version for colours)

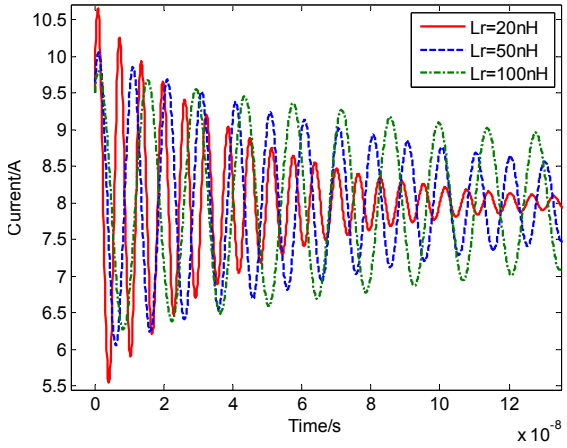
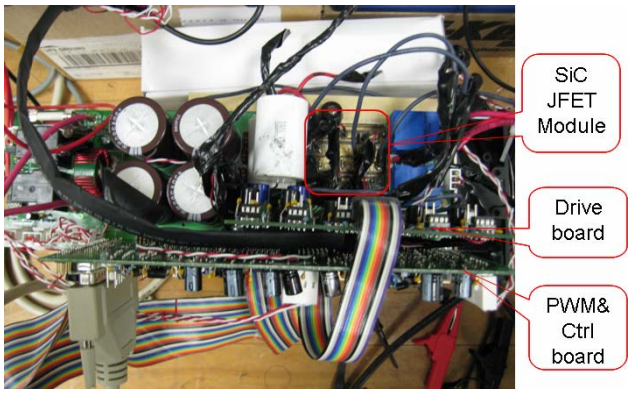
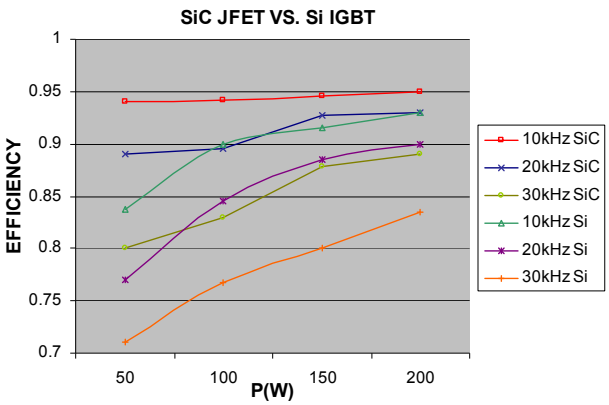



**Figure 7** Operation of the whole system, (a) 300 V prototype (b) efficiency comparison (see online version for colours)




(a)




(b)

## 5 Prototype and efficiency comparison

The final SiC-based inverter assembly is shown in Figure 7(a). In Figure 7(b), the efficiency of the SiC JFET-based inverter is compared to that of Si IGBT-based inverter. It can be seen that the efficiency of SiC JFET-based inverter is higher. It needs to point out that these experiments are carried out at low power ratings (300 V/200 W~1 kW). High power and high temperature experiments are needed to demonstrate further benefits of SiC JFET over Si IGBT.

## 6 Conclusions

This paper established a functional model of SiC JFET based on test results of the devices. The gate resistance is found to be of critical importance in the design of SiC JFET-based power converter circuits. Switch on oscillation and current spike caused by miller capacitance effect can also be eliminated by the appropriate design of gate resistance.

The measurement shows that the parasitic inductance has major impact on the switching oscillation. An optimised gate resistor can assure the SiC JFET to operate with fast switching speed and a safety range of dv/dt. In the next phase of study, high temperature operation, relevant thermal packaging (Jian et al., 2007) and large power ratings will be carried out to demonstrate the merits of SiC JFET.

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