# Design of *LLC* Resonant Converters Based on Operation-Mode Analysis for Level Two PHEV Battery Chargers

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***Abstract*—In this paper, the efficiency-oriented design considerations are discussed based on the operation-mode analysis of the *LLC* converter considering the characteristics of charging profiles. The mode boundaries and distribution are obtained from the precise time-domain model. The operation modes featuring both-side soft-switching capability are identified to design the operating trace of the charging process. Then the design constraints for achieving soft switching with the load varying from zero up to the maximum are discussed. Finally, a charging trajectory design methodology is proposed and validated through experiments on a prototype converting 390 V from the dc power source to the battery emulator in the range of 250–450 V at 6.6 kW with a peak efficiency of 97.96%.**

***Index Terms*—Battery, battery charger, dc–dc converter, electric vehicle, *LLC* resonant converter, plug-in hybrid electric vehicle (PHEV), resonate converter, zero-current switching (ZCS), zero-voltage switching (ZVS).**

## I. Introduction

With the depletion of fossil fuel reserves and the increase in greenhouse gas emissions, the research and development of plug-in hybrid electric vehicles (PHEVs) and pure electric vehicles (EVs) have been carried intensively [1]–[4]. In today's PHEVs and EVs, an on-board charger is installed to charge the high-power lithium-ion battery pack through the utility power [5], [6].

According to a thorough survey, the most common EV/PHEV charger architecture consists of a boost-type ac–dc converter for active power factor correction (PFC) and an isolated dc–dc converter as the second stage as shown in Fig. 1(a) [7]–[10]. The characteristic of this type of charger is mainly dependent on the dc–dc stage since the output voltage and current are regulated in this stage. Therefore, an efficient and compact isolated dc–dc converter is one of the most important topics for EV and PHEV battery charger. The *LLC* resonant converter with soft-switching capability for a wide operating range is considered to be a favorable topology to achieve both high efficiency and high-power density [11].

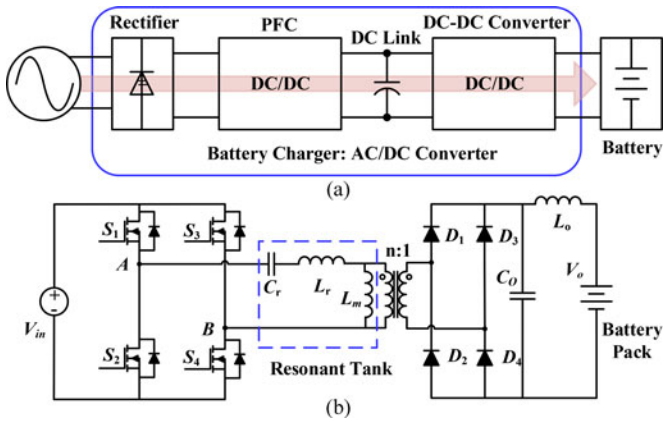


Fig. 1. Full-bridge *LLC* resonant converter. (a). Typical EV/PHEV charger system. (b). *LLC* dc–dc converter stage for the EV/PHEV charger.

A typical schematic of a full-bridge *LLC* resonant dc–dc converter used in EV/PHEV charger applications is shown in Fig. 1(b). The resonant tank consists of three reactive components: $L_r$ and $C_r$ in series, and $L_m$ in parallel with the primary of an $n$:1 ideal transformer. $C_r$ denotes the resonant capacitor, $L_m$ is the magnetizing inductance, and $L_r$ is the leakage inductance reflected in the primary side. The *LLC* converter modifies the gain characteristics of a series resonant converter (SRC) by utilizing the transformer magnetizing inductance to form multiple resonant stages. It greatly improves the light-load efficiency and allows the boost mode operation. However, its multiple resonant stages and various operation modes make it difficult to design [12].

Many design methodologies are proposed for this converter in the past decades. Exact analysis of *LLC* resonant converters [13] ensures accuracy but cannot be easily used to get a handy design procedure due to the complexity of the model. The first harmonic approximation (FHA) analysis [14] gives quite accurate results for operating points at and above the resonance frequency of the resonant tank [15], and has been widely used in constant output voltage applications where the *LLC* converter is designed to work at resonance at nominal condition. Designing a wide output range *LLC* resonant converter based on FHA method is investigated in [16]. The expanded range is mainly designed

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in frequencies above the resonant frequency. The secondary rectifiers' zero-current switching (ZCS) operation only appears in light-load condition in this region, which causes additional diode reverse losses compared to the region below resonance [17]. The accuracy of the FHA is barely satisfactory for optimal design in the below-resonance region. Optimal design methods are developed based on operation-mode analysis in [18], [19], and these approaches can give fairly good design results but call for utilizing sophisticated calculation tools. A simple yet accurate design oriented model and step-by-step design procedure that ensure most merits of *LLC* converter is presented in [20]. As an extension of [20], another design methodology for optimal efficiency by minimizing the reactive energy is presented in [21], but it involved solving nonlinear equations. Recently, an efficiency-oriented and straightforward design flow without recursive loop is developed in [22] based on the operation-mode analysis method presented in [17].

In the previous literatures, the load is usually assumed to be a pure constant resistor and the output is usually fixed. The wide voltage gain range is normally required to resist the input variation or to meet the holdup time [11], [23]. However, the design requirements of an *LLC* converter for a high voltage lithium-ion battery charger can be distinguished from the aforesaid applications. First of all, the non-linear load *i-v* characteristics related to the charging profile exist in the design of a resonant converter for battery charger applications. Second, not only the voltage ripple coming from the front-end stage needs to be resisted, but the output voltage also varies significantly in the whole charging process. In addition, the *LLC* converter should be able to handle a wide adjustable regulated output voltage range even when the load current varies. Third, the charge process for a lithium-ion battery usually contains several stages, and the output voltage and the load power change significantly during the whole charging process. It may go through different combination of no-load, full-load, and light-load conditions according to the control of the battery management system. Hence, high efficiency should be maintained in different load conditions. As a result, it is inappropriate to pick just one load condition out of the whole charging process to be the nominal condition to be targeted, which is normally done in the resistive load applications. The whole operating trajectory has to be taken into account for an optimal design.

In this paper, the time-domain model of *LLC* converter is introduced first. The operation-mode characteristics and the mode distribution are discussed and summarized in Section II. The operation modes that promised both-side soft switching are identified to be targeted. Based on the charging profile, the whole charging process is projected to the operation-mode distribution domain as operating trajectories in Section III. The key parameters and constraints that lead to the desirable charging trajectory are investigated in Section IV. Then the design procedure is proposed in Section V. Experimental results are presented in Section VI, and the conclusions are drawn in Section VII.

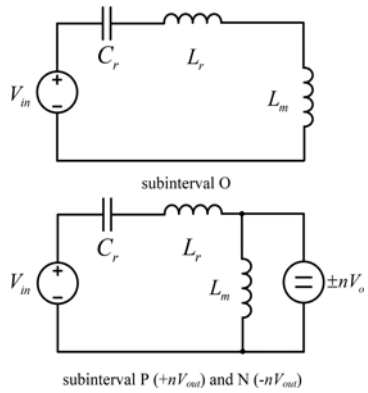


Fig. 2. Intervals of the *LLC* converter.

TABLE I
ABBREVIATIONS AND NORMALIZATIONS

| Circuit Variable | SYMBOL | Normalized Variable |
|---|---|---|
| Resonant frequency | $\omega_0 = 1/\sqrt{L_r C_r} = 2\pi f_0$ | – |
| Characteristic impedance | $Z_0 = \sqrt{L_r/C_r}$ | – |
| Inductance ratio | $l = L_r/L_m$ | – |
| Voltage gain | $M = nV_o/V_{in}$ | – |
| Time | $t$ | $\theta = \omega_0 t$ |
| Second resonant frequency | $\omega_1 = 1/\sqrt{(L_r + L_m)C_r}$ | $k = \omega_1/\omega_0$ |
| Switching frequency | $f_s = 1/T_s$ | $f_n = f_s/f_0$ |
| Half period | $1/2f_s$ | $\gamma = \omega_0/2f_s = \pi/F_n$ |
| Resonant capacitor voltage | $v_{Cr}(t)$ | $m_{Cr}(\theta) = v_{Cr}(t)/V_{\rm in}$ |
| Series resonant inductor current | $i_{Lr}(t)$ | $j_{Lr}(\theta) = i_{Lr}(t)Z_0/V_{\rm in}$ |
| Magnetizing inductor current | $i_{Lm}(t)$ | $j_{Lm}(\theta) = i_{Lm}(t)Z_0/V_{\rm in}$ |
| Magnetizing inductor voltage | $v_{Lm}(t)$ | $m_{Lm}(\theta) = v_{Lm}(t)/V_{\rm in}$ |
| Reflected output voltage | $nV_o$ | $M$ |

## II. MAIN FEATURES OF *LLC* RESONATE CONVERTERS

### A. Analysis in the Time Domain

Because the switching action exists in both the input switches and the output rectifier bridge, the *LLC* resonant converter represents a nonlinear and time-variant system, which makes the analysis complicated. However, by dividing the circuit operation into different subintervals, the converter can be described between transitions [21]. From symmetrical condition of the resonant converter, the steady-state can be characterized by a half period of operation. During the positive half switching cycle in which $S_1$, $S_2$ are turned ON, the converter can be described by three equivalent circuits as shown in Fig. 2. The capital letters O, P, and N are used to denote the three different subintervals, which is characterized by the voltage polarity (off, positive, and negative) across the magnetizing inductor $L_m$ [17]. The parameter *n* is the transformer turns ratio.

The subinterval O happens when the output is blocked by the diode rectifier, which forces the magnetizing inductor $L_m$ to participate in the series tank's resonance. Following the basic principles of circuit theory together with the normalizations in Table I, the normalized equations describing the resonant states are [13], [19], [24]

TABLE II
OPERATION MODES OF *LLC* RESONANT CONVERTER

| | $f_n < 1$ | | | | | $f_n = 1$ | | | $f_n > 1$ | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\theta$ | Mode PN | Mode PON | Mode PO | Mode OPO | Mode O | Mode P | Mode O | Mode NP | Mode NOP | Mode OP | Mode OPO | Mode O |
| $[0, \alpha)$ | P | P | P | O | O | P | O | N | N | O | O | O |
| $[\alpha, \beta)$ | N | O | O | P | $(\alpha = \beta)$ | $(\alpha = \beta)$ | $(\alpha = \beta)$ | P | O | P | P | $(\alpha = \beta)$ |
| $[\beta, \gamma]$ | $(\beta = \gamma)$ | N | $(\beta = \gamma)$ | O | $(\beta = \gamma)$ | $(\beta = \gamma)$ | $(\beta = \gamma)$ | $(\beta = \gamma)$ | P | $(\beta = \gamma)$ | O | $(\beta = \gamma)$ |
| Primary switches | ZVS/ ZCS | ZVS/ ZCS | ZVS | ZVS | ZVS | ZVS | ZVS | ZVS | ZVS | ZVS | ZVS | ZVS |
| Secondary rectifier | Hard switching | ZCS | ZCS | ZCS | OFF | ZCS | OFF | Hard switching | Hard switching | ZCS | ZCS | OFF |
| Conduction continuity | CCM | DCM | DCM | DCM | OFF | CCM | OFF | CCM | DCM | DCM | DCM | OFF |
| Voltage gain | Buck and boost mode | | Boost ($M > 1$) mode | | Cutoff mode | Unity ($M = 1$) mode | Boost mode | | Buck ($M < 1$) mode | | | Cutoff mode |
| Load condition | Heavy → Light | | | | | Independent | Light | | | Heavy → Light | | |
| Unknowns at given $F_n$, l and $P_n$ | $[j_{Lr}(0), m_{Cr}(0), \alpha, \beta, M]$ | | | | | | | | | | | |

$$m_{C_r,\mathrm{O}}(\theta) = [m_{C_r,\mathrm{O}}(0) - 1]\cos(k\theta) + \frac{1}{k} j_{L_r,\mathrm{O}}(0)\sin(k\theta) + 1 \quad (1)$$

$$j_{L_r,\mathrm{O}}(\theta) = k\,[1 - m_{C_r,\mathrm{O}}(0)]\sin(k\theta) + j_{L_r,\mathrm{O}}(0)\cos(k\theta) \quad (2)$$

$$j_{L_m,O}(\theta) = j_{L_r,O}(\theta) \quad (3)$$

$$m_{L_m,\mathrm{O}}(\theta) = \frac{1}{1+l}\,[1 - m_{C_r,\mathrm{O}}(\theta)] \quad (4)$$

with unknown starting values $m_{C_r,\mathrm{O}}(0)$ and $j_{L_r 0,O}(0)$. It is to be noted that in charger applications, the input voltage ripple is negligible compared to the wide output voltage range. So the input voltage should be chosen as the base voltage in the normalization rather than the widely changed output, which is different from the resistive load applications.

For the subintervals P and N, the rectifier bridge will conduct. The voltage across the magnetizing inductor is positive clamped and negative clamped, respectively, $m_{Lm}(\theta) = \pm M$. Therefore, the normalized waveforms for these subintervals can be identified as

$$m_{C_r,\mathrm{P/N}}(\theta) = (1 \mp M)(1 - \cos\theta) + m_{C_r,\mathrm{P/N}}(0)\cos\theta + j_{L_r,\mathrm{P/N}}(0)\sin\theta \quad (5)$$

$$j_{L_r,\mathrm{P/N}}(\theta) = \left[1 \mp M - m_{C_r,\mathrm{P/N}}(0)\right]\sin\theta + j_{L_r,\mathrm{P/N}}(0)\cos\theta \quad (6)$$

$$j_{L_m,\mathrm{P/N}}(\theta) = j_{L_m,\mathrm{P/N}}(0) \pm Ml\theta \quad (7)$$

$$m_{L_m,\mathrm{P/N}}(\theta) = \pm M \quad (8)$$

where $m_{C_r,\mathrm{P}}(0)$, $j_{L_r,\mathrm{P}}(0)$, and $j_{L_m,\mathrm{P}}(0)$ are used to denote the unknown initial conditions of subinterval P while $m_{C_r,\mathrm{N}}(0)$, $j_{L_r,\mathrm{N}}(0)$, and $j_{L_m,\mathrm{N}}(0)$ are for the subinterval *N*.

### *B. Operation Modes and Distribution Analysis*

According to analysis and simulation, a total of nine operation modes can be found by combining the intervals in different sequences. The operation modes can be named by the appearance order in which the subintervals occur in a half period. For instance, PO mode means that the subinterval P maintains for $\theta \in [0, \alpha)$ and it is followed by subinterval O for the rest of the half cycle ($\theta \in [\alpha, \gamma)$). All the operation modes and their characteristics are summarized in Table II. It can be seen that the main power interval P occurs in every half period except for the O mode under zero-load condition. So O mode is regarded as the cutoff mode since no power is delivered to the output [13]. There are six major operation modes (PN, PON, PO, OPO, NP, and NOP) that can be observed above the second resonant frequency when the operating frequency and load condition varies. Meanwhile, there are another two special modes that only happen at the specific conditions, which are P mode at resonant frequency and the OP mode at the boundary between NOP and OPO mode [17].

Each operation mode is constrained by several conditions. First, as the capacitor voltage and inductor current should be continuous, i.e., their values should be the same at the joints of adjacent subintervals. So it is intuitive that the continuity constraint conditions should be met. Second, by symmetry, the end values of the capacitor voltage and inductor current in the last subinterval should be opposite to their initial values of the first subinterval in steady state. Third, the magnetizing current and resonant tank current are the same at the end of the subinterval P or N when entering the next subinterval. In addition, the voltage across the magnetizing inductor should at least resonate to the output voltage at the end of subinterval O if it is followed by subinterval P or N [15]. If *X*, *Y* are assigned to denote the two different adjacent subintervals, and *B*, *E* are used to indicate the start subinterval and the end subinterval, respectively, in a half cycle, the aforementioned constraint conditions can be listed as Table III.

Since the load is disconnected from the resonant tank in subinterval O, the energy can only be delivered in subintervals P and

TABLE III
GENERAL CONSTRAINT CONDITIONS OF OPERATION MODES

| Constraints | Expressions |
|---|---|
| Continuity conditions | $m_{Cr,X}(\theta_{X,\mathrm{end}}) = m_{Cr,Y}(0)$<br>$j_{Lr,X}(\theta_{X,\mathrm{end}}) = j_{Lr,Y}(0)$<br>$j_{Lm,X}(\theta_{X,\mathrm{end}}) = j_{Lm,Y}(0)$ |
| Symmetry conditions | $m_{Cr,B}(0) + m_{Cr,E}(\gamma) = 0$<br>$j_{Lr,B}(0) + j_{Lr,E}(\gamma) = 0$<br>$j_{Lm,B}(0) + j_{Lm,E}(\gamma) = 0$ |
| Inductor current condition | $j_{Lr,P/N}(\theta_{P/N,end}) - j_{Lm,P/N}(\theta_{\mathrm{P/N,end}}) = 0$ |

TABLE IV
BOUNDARY CONDITIONS OF OPERATION MODES

| Boundaries | Solve as | Extra constraints |
|---|---|---|
| PN/PON | PN | $m_{Lm,\mathrm{N}}(\alpha) = -M$ |
| PON/PO | PO | $m_{Lm,\mathrm{O}}(\gamma) = -M$ |
| PO/OPO | PO | $m_{Lm,\mathrm{O}}(0) = M$ |
| OPO/NOP | OP | $m_{Lm,\mathrm{O}}(\alpha) = M$ |
| NOP/NP | NP | $m_{Lm,\mathrm{N}}(\alpha) = M$ |
| O | O | $m_{Lm,\mathrm{O}}(\gamma/2) = M$ |
| P | P | $M = 1$ |
| Peak gain of PON | PON | $j_{Lr,P}(0) = j_{Lr,\mathrm{N}}(\gamma) = 0$ |
| Peak gain of PN | PN | $j_{Lr,P}(0) = j_{Lr,\mathrm{N}}(\gamma) = 0$ |

N. Therefore, the normalized output power is derived as [13]

$$P_n = \frac{nV_o\overline{I_o}}{(V_{\mathrm{in}})^2/Z_0} = M\overline{j_o} = \frac{M}{\gamma}\int_{\theta_{P,0}}^{\theta_{P,\mathrm{end}}}\left[j_{Lr,\mathrm{P}}(\theta) - j_{Lm,\mathrm{P}}(\theta)\right]d\theta + \frac{M}{\gamma}\int_{\theta_{N,0}}^{\theta_{N,\mathrm{end}}}\left[j_{Lm,N}(\theta) - j_{Lr,N}(\theta)\right]d\theta. \quad (9)$$

Generally, the continuity conditions are used with (1)–(8) to get the intermediate values $x(\alpha)$ and $x(\beta)$ from the preceding subintervals. The normalized phase angle $\alpha$ and $\beta$ are used to denote the switching moment of adjacent subintervals. Then they are substituted into the following subinterval as its initial values. Finally, the final values $x(\gamma)$ at half period of an operation mode can be expressed by the corresponding initial values $x(0)$ of this mode. By applying the symmetry and inductor current conditions at given $P_n$ defined as (9), knowing $f_n$ and $l$, sufficient number of equations can be found to solve for the unknown variables as listed in Table I. However, the analytical solutions can only be found under cutoff mode and continuous conduction modes (CCMs), which, including O, P, PN, and NP. The discontinuous conduction modes (DCMs), which have been summarized in Table I, involve nonlinear equation solving. Hence, a numerical-based computing tool is required. To avoid the complexity in solving all the voltage gain characteristic curves, the boundaries of different operation modes can be done first to provide essential insight into the gain characteristic with parameters and load variation. The boundary curves are actually mode edges, which can be seen as a critical case of one of the six major modes or a particular boundary mode [17]. Since a boundary condition can be applied as an extra constraint, the mode equations can be solved without knowing $P_n$. For instance, the boundary of PO and PON mode is the solutions of PO mode satisfying the condition that the value of $m_{L_m}$ at the end of subinterval O is –*M*. Subinterval N is unavoidable before half cycle ends if this lower limit is exceeded. All the boundary conditions have been summarized in Table IV. The distribution of the operation modes is plotted by solving these boundary mode equations using MATLAB function fsolve(*x*).

As shown in Fig. 3, the distribution of the operation modes in a range of switching frequency and gain is mainly determined by parameter *l*. A shrinking effect, which means all the boundary curves distribute in a smaller frequency range with higher gain values, can be observed by increasing the value of *l*. Notably, all the boundaries of active modes converge to unity gain at $f_n = 1$, which confirms the load independent characteristic at resonance. In addition, the peak gain occurs in PN and PON mode and the curves converge to the peak of PN edge at the corresponding frequency.

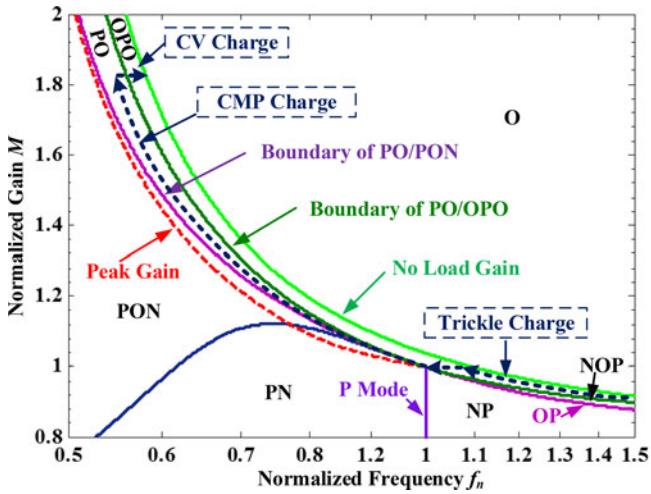


Fig. 3. Gain–frequency mode boundaries of *LLC* resonant converter with $l = 0.2$.

Based on the aforementioned analysis, the *LLC* resonant converter can be described and solved precisely as long as the operation conditions are known. The characteristics and distribution of operation mode provide importance design guideline for different applications.

## III. DESIGN CONSIDERATION OF *LLC* CONVERTER FOR PHEV BATTERY CHARGER

### A. Charging Profiles and the Operation Trajectory

The charge rate of a battery charger should be controlled according to the charging profile and the battery condition. As shown in Fig. 4, there are usually three stages in a typical charging profile of a high-voltage battery pack. A trickle charge stage with a constant current of 10% rated value ($I_0$) is performed first when the battery is deeply depleted. Bulk charge is followed after the voltage has risen above the trickle charge threshold ($U_0$). Different constant current (in the range of 20%–100% rated

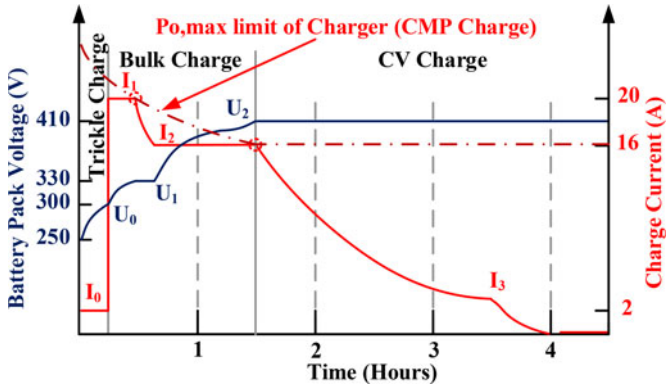


Fig. 4. Charging profile of a 410-V lithium-ion battery pack.

current) charge stages may exist in the Bulk charge stage due to the power limitation of the charger. Subsequently, the constant voltage stage is applied when the battery voltage reaches a certain value. Moreover, the charging actions may be modified as a response to the battery condition variation anytime. On the other hand, all kinds of charging profiles are requested for different battery packs, but all the profiles should be compromised with the maximum output power of the converter. So maintaining the maximum power output during the whole charge process (at minimal input voltage), which is referred as constant maximum power (CMP) charging profile in this paper, is reasonable to be seen as the overall charging profile, though it is not practical due to the safety and long cycle life consideration [25].

In this case, the *LLC* converter actually starts with a light-load operation at the lowest gain. Then it goes through the full-load operation within a wide gain range. The transition from full load back to light-load operation occurs at the highest gain gradually. Besides, no-load operation may happen at any stage dependent on the battery status.

Soft switching is the most desirable advantage of resonant converters because it reduces switching loss and EMI. *LLC* topology is capable of realizing zero-voltage switching (ZVS) for input inverting choppers and ZCS for output rectifiers at the same time [27], which minimizes the switching losses of the MOSFETs and diodes. Therefore, from a designer's point of view, the charger design target is to achieve soft switching under all operating conditions, as well as no-load operation ability. It has been summarized in Table II that there are several operation modes feature with primary ZVS and secondary ZCS capability: OPO, OP, P, and PO modes. Particularly, PON mode also holds the both-side soft-switching ability when the operation point locates in the zone formed by peak gain curve and the PON/PO boundary shown in Fig. 3. Among these candidates, OPO mode can be operated as both buck mode and boost mode at light-load condition. So it is suitable for the trickle charge stage and the CV charge stage. As for the CMP charge stage, a larger charging current is needed when the battery voltage is low. Hence, the equivalent load is relatively heavier at the beginning of the CMP charge. Hence, the P mode, which features a load independent characteristic, is suitable for the start point of the CMP charge stage. So far, PO mode and PON mode are left to be targeted for the rest part of the CMP charge. The peak gain points in the PON mode form the critical boundary of realizing primary ZVS operation. So the peak voltage gain in a specific design is usually picked as design point since it indicates the converter's voltage regulation capability at the lowest permissible operating frequency. However, the most important feature of peak gain mode is that the switching current equal zero as summarized in Table IV. In practice, the switching current should be slightly larger than zero for reliable ZVS of the MOSFETs. In consequence, peak gain points in PON mode are not likely to be the best choice to operate at the required peak output voltage condition, let alone its complexity to be solved. In comparison, the entire PO mode is within both-side soft-switching region. The gain in PO mode increases monotonically with the decrease of operating frequency, which ensures the control stability in the controller design [18]. Besides, when the inductance ratio is larger, the energy stored in the magnetizing inductor is lower due to the reduced circulating tank current. This part of energy will be released faster during the N subinterval of PON mode, which causes the PO/PON boundary getting closer to the peak gain curve and finally intersecting at a certain low frequency. Therefore, PO mode is the most preferable boost operation mode. Meanwhile, the PO/PON boundary can be regarded as a more practical gain limitation curve than the accrual peak gain curve to ensure soft-switching operation. Last but not least, O mode exists in the whole frequency and gain range at no-load condition as summarized in Table II and shown in Fig. 3, which ensures the charging can be shut down at any battery voltage due to charging completion or a fault detection.

Based on the aforementioned analysis, a possible operation trajectory that promises soft switching under all charging stages can be plotted in Fig. 3 (dotted line with arrow). It can be seen that the trajectory start with O mode at the highest frequency waiting for the charging command. It goes through OPO mode above resonance during trickle charge stage. The CMP charge stage is initiated from P mode to take advantage of its load independent property. By proper designing parameters, the whole CMP charge stage can be restricted within the PO mode region. In CV charge stage, the converter maintains the highest required voltage gain while the equivalent load decreases gradually and ends with O mode eventually.

In addition, to further confirm the possibility of the proposed operation trajectory, the boundaries and distribution of the normalized load power of operation modes are plotted in Fig. 5. The corresponding preferable operation trajectory in Fig. 3 is also plotted in power–frequency and power–gain mode distribution coordinates respectively. As can be seen, the whole CMP charge can be limited in PO mode region as long as the normalized rated output power $P_{n,\mathrm{full}}$is designed between $P_{n,\max}$and $P_{n,\min}$ as indicated in Fig. 5 for required gain within allowable frequency range. However, in order to locate the trickle charge trajectory within the OPO zone, the upper limit may be lower than $P_{n.\max}$. For instance, as mentioned, a constant 10% rated charge current is usually carried out in trickle charge stage, which means the normalized output power during this stage is about 1/10 of the rated output power. Therefore, the

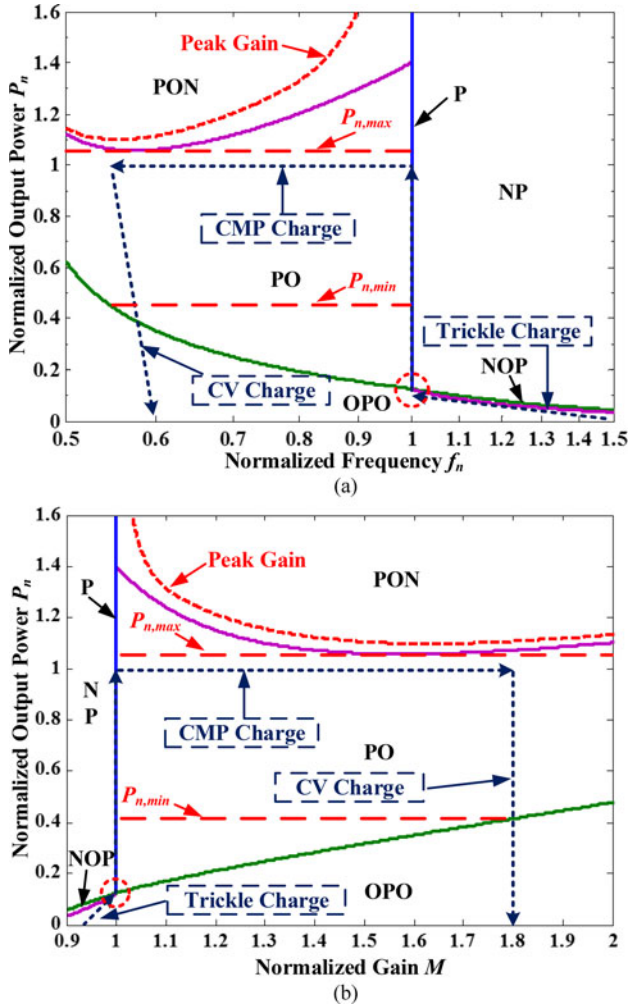


Fig. 5. *LLC* mode boundaries and distribution with $l = 0.2$. (a) Power–frequency distribution and the peak gain limit (the dashed line). (b) Power–gain distribution.

normalized power at the crossing point of P mode and OPO boundary, which is highlighted by dashed circle in Fig. 5, can be regard as the maximum value of $0.1P_{n,\text{full}}$. The actual upper limit is shown as the possible CMP charge trajectory in Fig. 5.

In CV charge stage, the output power decreases gradually while the gain maintains the same. So the trajectory of CV charge can also be drawn in Fig. 5.

## IV. Charging Trajectory Design

### A. Key Design Parameters

To design the *LLC* converter operating along the trajectory that offer the whole range with soft-switching capability during the charging process, the three key elements should be considered thoroughly: inductance ratio $l$, transformer turns ratio $n$, and characteristic impedance $Z_0$.

First of all, the unity gain operation is designed at the heaviest load condition when the CMP charge is applied to the battery pack at its lowest voltage. Therefore, the transformer turns ratio

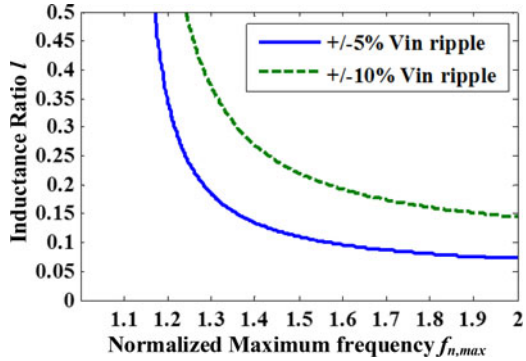


Fig. 6. Relationship between the inductance ratio and the normalized maximum frequency at no-load condition.

can be calculated by

$$n = \frac{V_{\text{in,nom}}}{V_{\text{out,min}}}. \tag{10}$$

After determining $n$, the minimum gain is given as

$$M_{\text{min},0} = \frac{nV_{\text{out,min}}}{V_{\text{in,max}}} = \frac{V_{\text{in,nom}}}{V_{\text{in,max}}}. \tag{11}$$

In general, the minimum gain occurs when the battery is at its lowest voltage and waiting for the charging command from the battery management system. The switching frequency should be adjusted to its maximum value to step down the output to ensure the no-load operation when the maximum input voltage is applied to the converter. In this case, the converter operates in O mode and the relationship between the variables can be solved analytically [26]. The inductance ratio is

$$l = \left(\frac{1}{M_{\text{min},0}} - 1\right)\frac{8f_{n,\text{max}}^2}{8f_{n,\text{max}}^2 - \pi^2}. \tag{12}$$

The mode distribution is determined once the inductance ratio is chosen. According to (11), the required minimum gain depends on the ripple of input voltage, which is actually the output ripple of the front-end PFC stage in the charger applications. As a result, the maximum operating frequency $f_{n,\text{max}}$ becomes the most important predefined parameter by the designer. Typically, the output voltage ripple of the boost-type PFC is $\pm 5\%$ to $\pm 10\%$. In this case, the relationship between $l$ and $f_{n,\text{max}}$ can be plotted in Fig. 6. As shown in Fig. 6, a smaller expected operating frequency range gives rise to higher inductance ratio. However, it has been found in [22] that the resonant tank RMS current tend to be lower as $l$ decreases at the same normalized load power $P_n$, which reduces the conduction losses. Further, this effect is notably weaken as $l$ is lower than 0.25. On the other hand, the available voltage gain in the same specific frequency range decreases with a smaller $l$. Therefore, the objective of the optimal design is to reduce the conduction loss while maintaining the required gain within frequency limitation.

As aforementioned, the PO/PON boundary can be regarded as a conservative design boundary for the primary ZVS realization of MOSFET-based inverters in some circumstances, especially when the PO/PON boundary is close to the peak gain boundary.

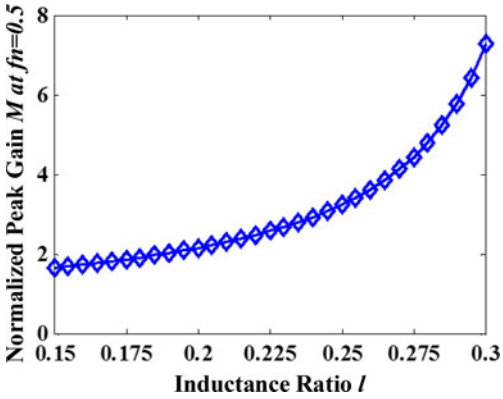


Fig. 7. Relationship between the peak gain limitation and inductance ratio at $f_{n_{\min}} = 0.5$.

And the efforts of reducing conduction losses prefer an $l$ value lower than 0.25, which makes the two boundaries close enough without losing any useful design region according to the aforementioned operation-mode analysis method (as can be seen in Fig. 3). So the gain of PO/PON boundary at the lowest operating frequency is reasonable to be the gain limitation. The gain limited by $l$ when $f_{n,\min} = 0.5$ can be drawn in Fig. 7. According to the aforementioned analysis, $l$ can be chosen based on the required maximum gain and the input voltage ripple by Figs. 6 and 7.

The next step is to select a suitable value for the characteristic impedance $Z_0$ once $l$ is determined. According to the definition of normalized rated load power

$$P_{n,\text{full}} = \frac{P_o}{(V_{\text{in,min}})^2} Z_0. \tag{13}$$

The normalized output power is proportional to $Z_0$ since the input voltage has been fixed by the front-end stage. So the locus of CMP charge actually depends on the characteristic impedance. Assigning different values to $P_{n,\text{full}}$, the variation of gain–frequency curve and CMP charge trajectory can be shown as Fig. 8. It can be seen that the gain curves are pushed towards the PO/PON boundary by increasing $Z_0$. And the CMP trajectories are also lifted towards the PO/PON boundary with a larger $Z_0$.

Obviously, a small $Z_0$ makes the *LLC* converter overqualified because the operation trace will be far away from the boundary. Besides, a larger $Z_0$ value is preferable motivated by reducing conducting losses. In theory, the bottom of the PO/PON boundary $P_{n,\text{PO/PON,min}}$ in Fig. 8(b) can be targeted as the rated normalized power $P_{n,\text{full}}$ to calculate the corresponding $Z_0$ value, since it ensures the whole CMP charging process located in PO operation region. This condition can be written as

$$Z_{o,\text{PON}} \le \frac{P_{n,\text{PO/PON,min}}}{P_o / V_{\text{in,min}}^2}. \tag{14}$$

However, three more constraints should be taken into account when designing $Z_0$.

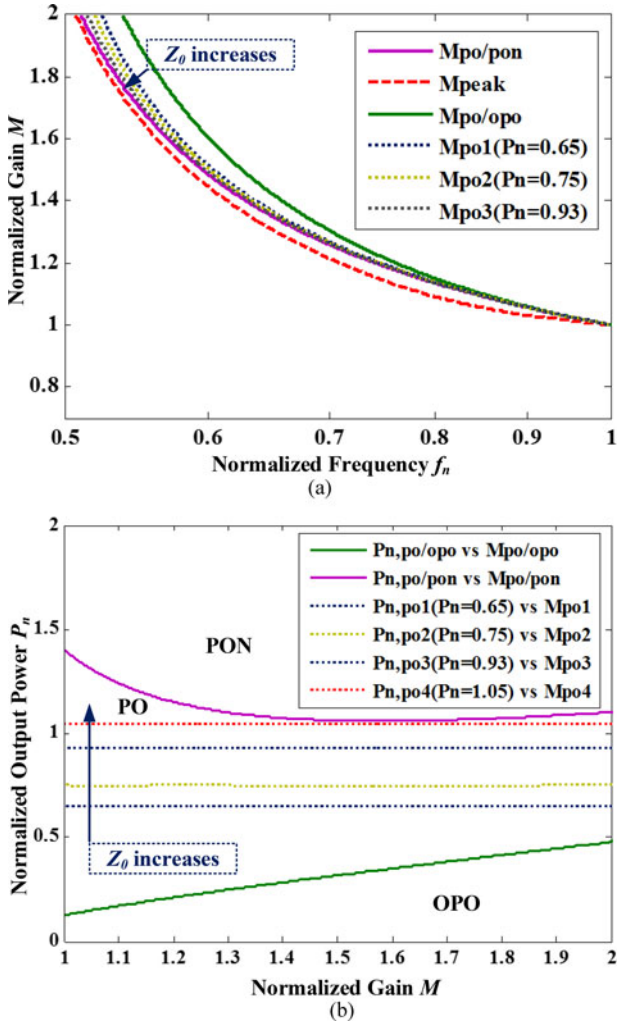


Fig. 8. (a) Normalized gain $M$ curves (dotted lines) for various designed $P_n$ values in PO region with $l = 0.2$. (b) CMP charge trajectories (dotted lines) for various designed $P_n$ values in PO region with $l = 0.2$.

### B. Design Constraints

The trickle charge only occurs when the battery is deeply depleted, which is normally supposed to be avoided for the sake of battery health [27]. However, it is still worth to have it benefit from the soft-switching operation, because the constraint can be easily combined into the whole design procedure. In the aforementioned, the normalized output power at the end of the trickle charge is about $0.1P_{n,\text{full}}$. This value should not be larger than the value of the OPO/NOP boundary at the resonant frequency to restrict the trace within OPO region as shown in Fig. 5. Consequently, the constraint condition can be expressed as

$$Z_{0,\text{TCK}} \le \frac{P_{n,\text{NOP/OPO}}\big|_{f_n=1}}{0.1P_o / V_{\text{in,min}}^2}. \tag{15}$$

Besides, the switching current, which is also the initial resonant inductor current $j_{L_r}$, $X(0)$ in each cycle, should be evaluated in different operation modes. Generally speaking, the worst-case situation for primary ZVS operation occurs when

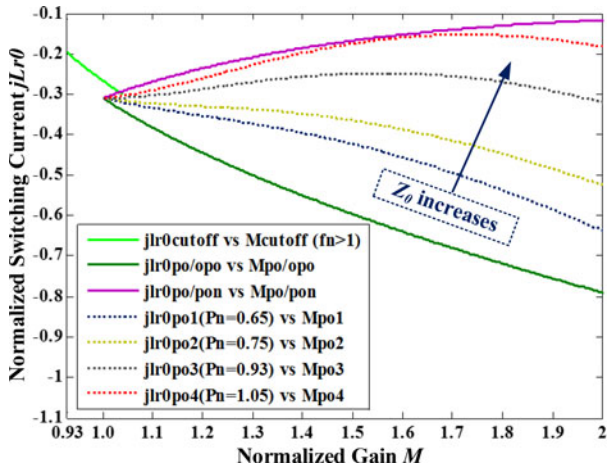


Fig. 9. Normalized switching current curve (dotted lines) for various designed $P_n$ values in PO region and cutoff mode above resonance with $l = 0.2$.

the output voltage is regulated at its minimum value, and the maximum input voltage is applied to the converter under the no-load condition. In this case, the switching frequency is usually regulated to its maximum value and the converter operates in the cutoff mode. At this time, the switching current should be considered as its smallest value globally to reduce the no-load conduction loss. On the other hand, this current has to be large enough to discharge the MOSFETs' junction capacitors within the dead time for soft-switching realization. The required minimum switching current $I_{\mathrm{sw,min}}$ is calculated according to the parasitic parameters of the selected MOSFET and the dead time. So the third constraint of $Z_0$ is given as

$$Z_{0,\mathrm{OSW}} \le \left| j_{L_r 0,O}\left(M_{\min}, f_{n,\max}\right)\right| \frac{V_{\mathrm{in,min}}}{I_{\mathrm{sw,min}}}. \qquad (16)$$

So far, there are three constraints applied to the selection of $Z_0$ in order to confine the *LLC* converter operating in the desirable modes and ensure the soft-switching capability. Based on (14)–(16), the upper limit of the characteristic impedance can be expressed as

$$Z_{0,\max} = \min\left\{Z_{0,\mathrm{PON}}, Z_{0,\mathrm{TCK}}, Z_{0,\mathrm{OSW}}\right\}. \qquad (17)$$

At last, the switching current variation is analyzed to verify if the primary ZVS operation has been promised under a certain designed $Z_0$. The variation of switching current in cutoff mode above the resonance should solved first, since the switching current at the maximum frequency (or at the lowest gain) is set to be the lowest value that ensures the parasitic capacitors of the MOSFETs can be fully discharged. The switching current variation of PO/PON and PO/OPO boundary can also be solved easily to draw the outline of the PO region. The variation of normalized switching current $j_{Lr_0}$ under different designed $P_{n,\mathrm{full}}$ value along the CMP charge trajectory can be shown in Fig. 9 when $l = 0.2$. In Fig. 9, the normalized switching current at the minimum gain ($M_{\min} = 0.9$) is –0.2, where negative means the tank impedance is inductive. Hence, the absolute value of the normalized switching current during CMP charge should be larger than 0.2 to guarantee the ZVS operation. Apparently, a larger $Z_0$ results in smaller switching current in the PO region. However, the normalized switching current does not always vary monotonically with the voltage gain, which makes it impossible to get a handy analytical constraint expression for $Z_0$ design as before. As shown in Fig. 9, the switching current increases with the gain when the designed normalized load power is between 0.65 and 0.75. But the monotonicity is lost in the range of 0.9–1.05. The absolute value of the normalized switching current decreases first and then goes up as the gain increases. The goal is to have ZVS operation when the output power is kept constant under different output voltage (gain). The criterion is that the switching current should never be smaller than the lower limit that has been set in the cutoff mode at minimum gain, which means 0.2 in Fig. 9. Although the design $P_{n,\mathrm{full}} = 1.05$ guarantees the PO operation as can be see in Fig. 8 (b), it does not ensure the switching current large enough to keep the ZVS characteristic. Because in this curve the absolute value of the normalized switching current is lower than 0.2 when the gain is higher than 1.4. That is to say, the maximum characteristic impedance calculated by (17) may not be qualified as the final design value.

As a result, one more step is necessary to draw the conclusion. The corresponding maximum normalized load power $P_{n,\max} = \left(P_o/V_{\mathrm{in}}^2\right) Z_{0,\max}$ calculated by (13) and (17) should be assigned to the PO mode equations to solve for the normalized switching current curve. If the plotted curve locates below the line $j = j_{L_r 0,O}\left(M_{\min}, f_{n,\max}\right)$, $Z_{0,\max}$ is eligible to be used. Otherwise, the $Z_0$ value needs to be reduced further to meet the criterion. With the accepted $Z_0$, the resonant circuit parameters are calculated as

$$L_r = \frac{Z_0}{2\pi f_0} \qquad C_r = \frac{1}{2\pi f_0 Z_0} \qquad L_m = \frac{L_r}{l}. \qquad (18)$$

## V. Design Procedure

The proposed design procedure for the PHEV battery charger application is illustrated in Fig. 10. This design method focuses on restricting the whole charging trajectory within the preferable operation modes that offer the converter with both-side soft-switching capability. The effort of minimizing the circulating energy has been made by two steps of crucial importance during the design process. First, the inductance ratio *l* is minimized according to the given required gain range. Second, it is further accomplished by searching the allowable maximum characteristic impedance $Z_0$ limited by several design constraints, which ensure reliable ZVS operation. Although these two optimization steps have induced two recursive loops in the whole design flow. The accuracy and the existence of solution can be promised by the precise time-domain model. In particular, for EV charger applications, the input ripple is fixed by the front-end stage ($\pm 5\%$ to $\pm 10\%$) and the output range depends on the specifications of the battery pack (typically 250–500 V). It has been found an $l$ value around 0.2 is able to cover this gain range within a reasonable frequency range ($f_{\mathrm{n}} = 0.5$–$1.6$) according to Figs. 6 and 7. The recursion number can be reduced greatly by starting from an experienced value. As for the second recursive loop, it is found that the switching current of the cutoff mode

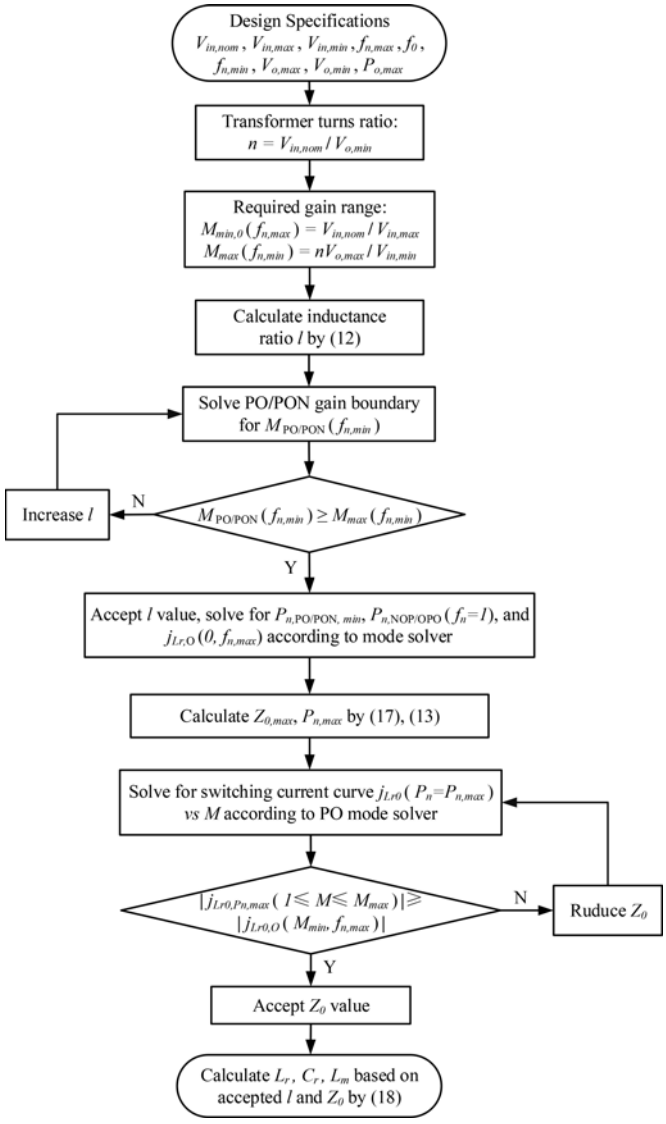


Fig. 10. Charging trajectory design procedure.

TABLE V
DESIGN SPECIFICATION FOR *LLC* RESONANT CONVERTER

| Parameter | Designator | Value |
|---|---|---|
| Input voltage range | $V_{in,\min} - V_{in,\max}$ | 370–410 V |
| Input voltage nominal | $V_{in,\text{nom}}$ | 390 V |
| Output voltage range | $V_{\text{out},\min} - V_{out,\max}$ | 250–450 V |
| Maximum output power | $P_{\text{out},\max}$ | 6.6 kW |
| Resonant frequency | $f_0$ | 155 kHz |
| Operating frequency range | $f_{s\min} - f_{s\max}$ | 85–200 kHz |

TABLE VI
COMPONENTS USED IN THE PROTOTYPE CONVERTER

| Component | Manufacturer | Part # |
|---|---|---|
| MOSFET | Infineon Technologies | IPW60R041C6 |
| Diode rectifiers | Fairchild Semiconductor | FFH60UP60S |
| Resonant film capacitors | EPCOS | MKP 20 × 3.3 (nF) MKP 1×2.2 (nF) |
| Magnetic ferrite core of transformer | TDK | PC40 EC90 × 90 × 30 |
| Litz-wire | HM Wire International | AWG38 × 1000 |
| Output film capacitors | Vishay | MMKP383 6 × 1($\mu$F) |

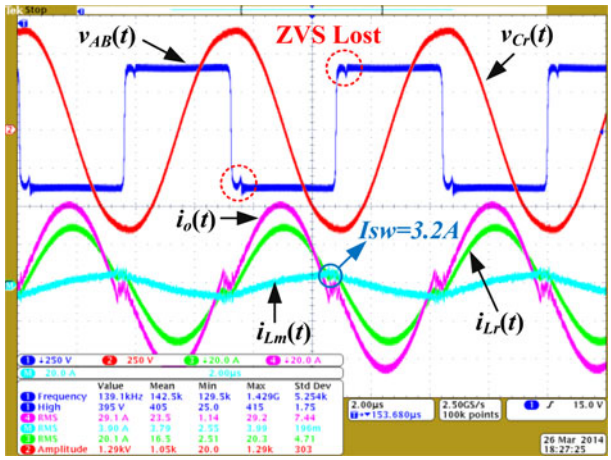


Fig. 11. Experimental waveforms of *LLC* converter prototype with the parameters skipping the last step of the procedure at $V_{\text{in}} = 390\,\text{V}$, $V_o = 280\,\text{V}$, and $P_o = 6.6\,\text{kW}$

at $f_{n,\max}$, which relies on the parasitic capacitance of the selected MOSFET, plays the most important role in designing $Z_0$. An appropriate estimation is helpful in reducing the number of recursion.

## VI. EXPERIMENTAL RESULTS

To demonstrate the proposed charging trajectory design method, a prototype of full-bridge *LLC* resonant converter for a level 2 charger based on specifications given in Table V was built. The semiconductor device and the key circuit components of the converter are listed in Table VI.

Following the proposed procedure, the turns ratio is calculated by (10) as 1.56. The inductance ratio is solved as $l = 0.1984$ from (12). The mode boundary and distribution solver mentioned in Section II is used to solved for the limitation of $Z_0$ set by (14)–(16). The calculated results are listed as follows: $P_{n,\text{PO/PON,min}} = 1.05$, $P_{n,\text{NOP/OPO}}(f_n = 1) = 0.1254$, $j\_L_r 0, O(M_{\min} = 0.9512, f_{\text{n,max}} = 1.29)| = 0.2185$. The corresponding constraints are: $Z_{0,\text{PON}} = 21.78$, $Z_{0,\text{TCK}} = 26.01$, $Z_{0,\text{OSW}} = 22.45$. It is to be noted that the minimum switching current $I_{sw,\min}$ in (16) is set to 3.6 A based on the parasitic parameters of the selected MOSFET. Therefore, the upper limit of $Z_0$ is chosen as 21.78 according to (17). So the upper limit is actually set by the PO/PON boundary $P_{n,\text{PO/PON,min}} = 1.05$ in this design example.

To verify the necessity of the second recursive loop of the proposed design procedure, the $Z_0$ calculated earlier is accepted as the final design value temporarily. The resonant tank parameters can be calculated by (18) as follows: $L_r = 22.36$ $\mu$H, $C_r = 47.14$ nF, and $L_m = 112.7$ $\mu$H. A resonant tank has

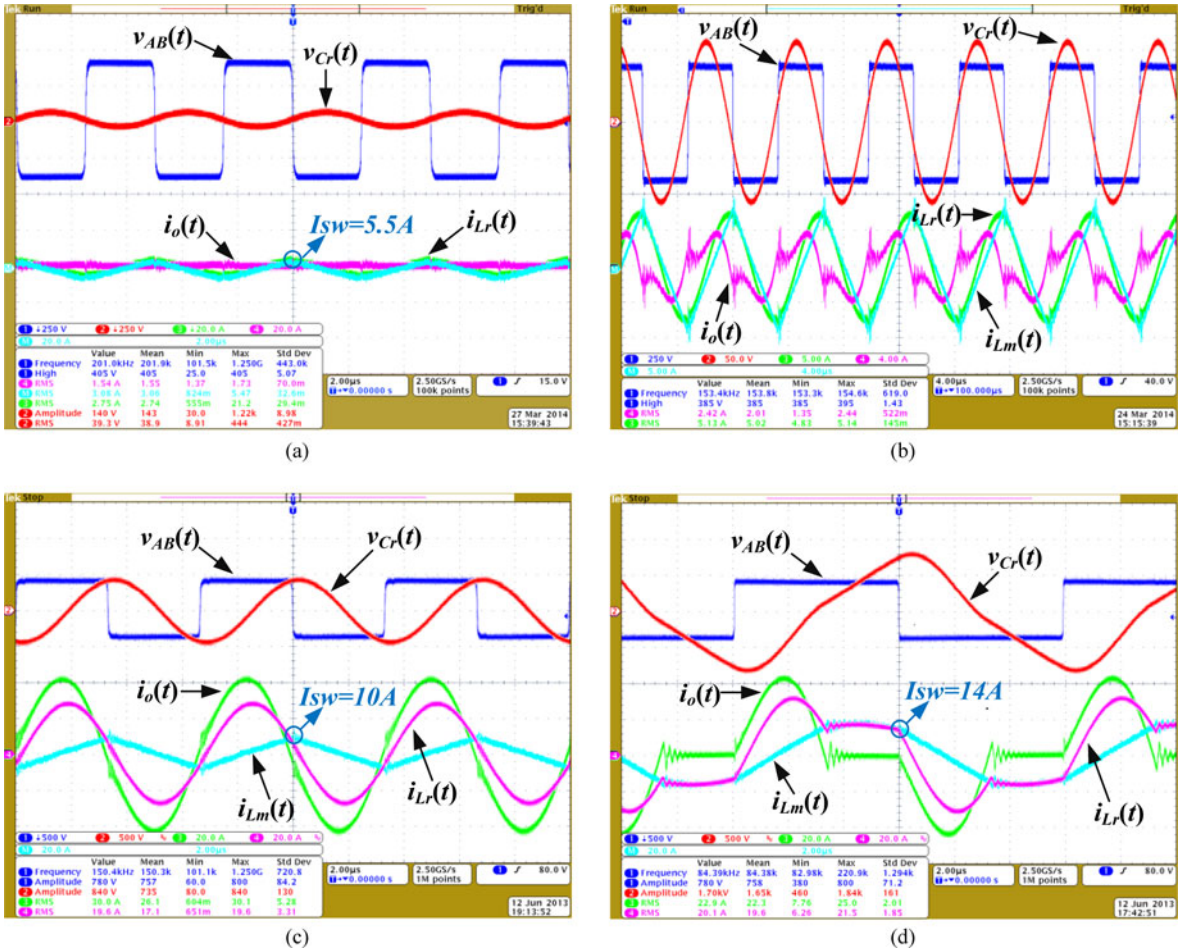


Fig. 12. Experimental waveforms of *LLC* converter: (a) no-load operation: $V_{\rm in} = 390\,V$, $V_o = 250\,V$, and $f_s = 201\,{\rm kHz}$. (b) OPO mode operation in trickle charge: $V_{\rm in} = 390\,V$, $V_o = 250\,{\rm V}$, $I_o = 2\,{\rm A}$, and $f_s = 153.4\,{\rm kHz}$. (c) P-mode operation at the beginning of CMP charge: $V_{\rm in} = 390\,{\rm V}$, $V_o = 250\,{\rm V}$, $P_o = 6.6\,{\rm kW}$, and $f_s = 150.4\,{\rm kHz}$. (d) PO-mode operation at the end of CMP charge: $V_{\rm in} = 390\,{\rm V}$, $V_o = 450\,V$, $P_o = 6.6\,{\rm kW}$, and $f_s = 84.19\,{\rm kHz}$.

been built and tested based on the aforementioned parameters at full-load conditions. The experimental waveforms are shown in Fig. 11. In this figure, $v_{AB}(t)$ denotes the voltage applied on the resonant tank. The voltage across the resonant capacitor is shown as $v_{C_r}(t)$. $i_{L_r}(t)$, and $i_{L_m}(t)$ are used to indicate the primary resonant tank current and the transformer magnetizing current respectively. The secondary current through the rectifier is indicated as $i_o(t)$. As predicted in Fig. 9, though the converter operates in the preferable PO mode, the switching current $I_{sw} = 3.2$ A (which is lower than the designed cutoff switching current 3.6 A) is not large enough to discharge the parasitic capacitors of the MOSFETs to ensure ZVS realization. An oscillation can be observed when the dead-time ended and gate drive signals are applied to the corresponding switches, which induces switching losses and should be avoided. Hence, the value of the characteristic impedance needs to be reduced further. The variation of the normalized switching current shown in Fig. 9 is used as a design reference since the designed $l$ is very close to 0.2. It can be seen that the switching current varies monotonically when the normalized output power is lower than 0.75. So it is chosen as the normalized rated output power for reliable ZVS operation. The resonant tank parameters are recalculated as follows: $L_r = 15.97\ \mu$H, $C_r = 66\,nF$, and $L_m = 80.51\ \mu$H. The actual measured values are given for comparison: $n_a = 1.58$, $l_a = 0.198$, $L_{r,a} = 15.3\ \mu$H, $C_{r,a} = 68.2$ nF, and $L_{m,a} = 77.3\ \mu$H. It is to be noted that the magnetic integration is adopted to downsize the resonant tank, which makes it not easy to adjust the parameters to fit the designed values exactly.

The operating trajectory during the whole charging procedure is verified first. Four special operating points are picked to confirm the accomplishment of the design target. The experimental waveforms of these operations are given in Fig. 12, in which the definitions of the symbols are the same as those in Fig. 11. First, the no-load operation $(i_o(t) = 0)$ at the lowest output voltage (250 V) is assured when the switching frequency is regulated to its maximum value (201 kHz) by Fig. 12(a). Second, the OPO mode operation can be observed in Fig. 12(b) when the output current is set around $0.1I_{o,\rm full}$ at 250 V output, which stands for the end of the trickle charge stage. The oscillation of $i_o(t)$ is caused by the parasitic capacitor of the output rectifier when they are cutoff from the resonant tank during the O subintervals of OPO mode. Third, the maximum output power

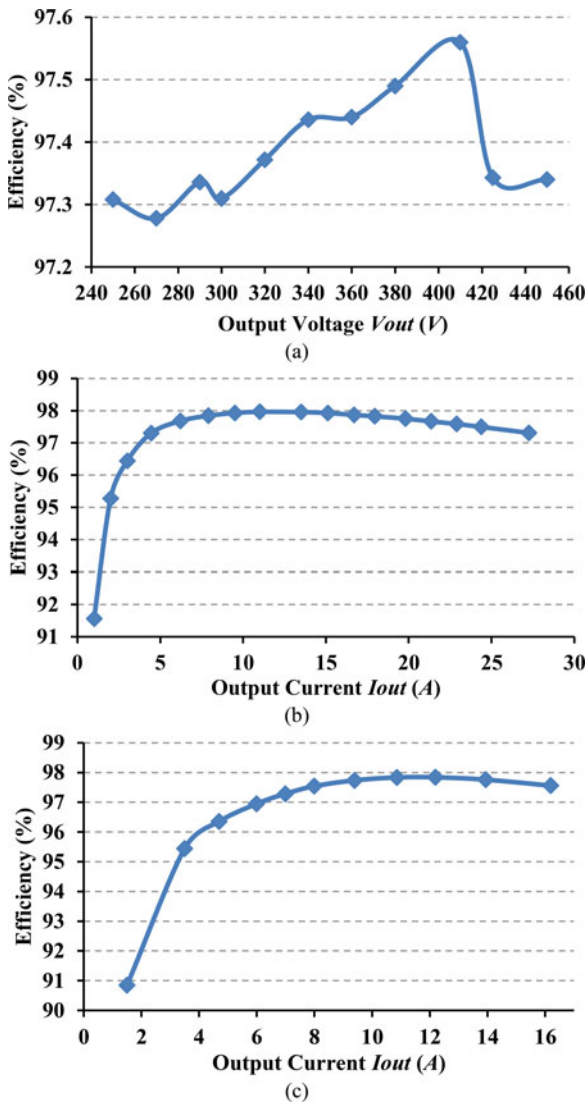


Fig. 13. *LLC* converter prototype performance: (a) Measured efficiency versus output voltage at $P_o = 6.6\,\mathrm{kW}$ and $V_{\mathrm{in}} = 390\,\mathrm{V}$. (b) Measured efficiency versus output current at $V_o = 250\,\mathrm{V}$ and $V_{\mathrm{in}} = 390\,\mathrm{V}$. (c) Measured efficiency versus output current at $V_o = 410\,\mathrm{V}$ and $V_{\mathrm{in}} = 390\,\mathrm{V}$.

is delivered at 250 V output voltage while P mode operation is promised as shown in Fig. 12(c). So the heaviest load condition is designed at the load independence mode. Last, the typical PO mode operation waveforms can be seen in Fig. 12(d) when the output voltage is regulated to the maximum value 450 V while the maximum output power is transferred, which indicates the whole CMP charge is restricted within the PO region. In addition, it can be concluded from Fig. 12 that both-side soft switching is realized since the charging trajectory is going along the desirable trace in the preferable region.

The performance of the CMP charge is tested. An electronic load is used to simulate the load characteristic of the battery pack in the experiments. The efficiency of the converter as a function of output voltage for CMP charge is shown in Fig. 13 (a). It can be seen that the efficiency is higher than 97.2% during the whole CMP charge stage and hits the peak at 410 V output with 97.56%. The efficiency curves of the CV charge stage at 250 and 410 V output are also given in Fig. 13(b) and (c) for the light-load performance evaluation. It can be seen that the conversion efficiency maintains above 90% from 10% load to full load. The peak efficiency of 97.96% is exhibited at output current of 11 A at 250 V (2.75 kW).

## VII. Conclusion

The *LLC* resonant converter applied in EV/PHEV battery charger systems has been analyzed, and the design methodology is presented. Different from the resistive load applications, which come along with a single nominal condition, full-load operation is required in a very wide output voltage range for battery chargers. So it is a trajectory design target rather than a single point design target. The mode boundaries and distribution of *LLC* converter are discussed in the need of locating the operation trace to the preferable region. The key parameters that affect the designed operating trajectory are identified. Finally, all the discussion has led to a design procedure that ensures soft switching under all operating conditions. A 6.6 kW, 390 V dc input and 250–450 V output *LLC* converter is built using the proposed method, which achieves 97.96% peak efficiency. The future research will be focused on the power density improvement by optimal transformer design and a straightforward design procedure without recursive loops.

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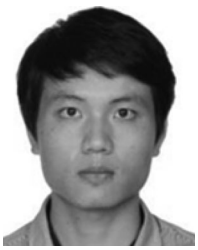

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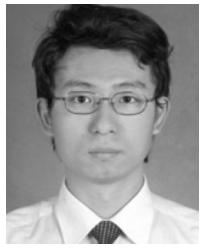

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