

A Novel Bidirectional Flying Inductor-Based Converter for Dual-Purpose Application

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Abstract—This paper presents a new flying inductor-based converter as a power electronics interface suitable for application in both DC or single-phase AC grids using the same terminals. This topology does not need to have a mid-point of DC sources or DC-bus capacitors at the input side of the inverter and only have one main inductor to transfer energy. Therefore, the power density of the proposed converter is extremely high, achieving 4.7 W/cm^3 at 5 kW. The voltage boosting feature in a single-stage and operation in a wide range of input DC power supply is the other benefit of the proposed solution. Since electrolytic capacitors are not used in the structure, the life of the converter is increased. The operation modes of the converter are explained in detail. To verify the performance of the proposed topology, a prototype (2.5 kW/5 kW) was built and tested in the laboratory. The related experimental results are presented.

Index Terms—Flying-inductor converter, dual-purpose application, single-stage, voltage boosting.

I. INTRODUCTION

THE growing global energy demand underscores the urgency of developing new energy sources. By 2050, electricity consumption is projected to rise by 22% in residential sectors and 32% in industrial sectors [1]. To sustainably meet this growing demand, renewable energy sources (RESs) like solar and wind power must play a significant role in addressing the increased energy requirements. However, the existing electrical infrastructure is not well-equipped to accommodate the large-scale integration of RESs. As a result, energy storage systems are regarded as a crucial solution for maintaining grid stability in scenarios with high RES penetration. Meanwhile, it is estimated that 1.9 million electric vehicle battery (EV) packs will be retired by 2040. While no longer suitable for powering EVs, these batteries remain viable for use in energy storage systems [2], [3]. Consequently, extensive research has been focused on the second-life utilization of these batteries for energy storage applications [4], [5], [6].

As most RESs and battery storage systems are DC-based, many researchers have recently focused considerable attention on DC microgrids [7], [8], [9]. From the technical perspective, DC grids offer several advantages over ac grid. For instance, ac grids must contend with challenges such as voltage, frequency, and phase angle synchronization, harmonic suppression, and reactive power compensation, none of which are issues for DC grids. Furthermore, DC grids are inherently more compatible with RESs, battery storage systems, and electric charging system. With the development of power electronics converters in recent decades, DC grids can be implemented using advanced DC-DC converters at any voltage level [10], [11],

[12]. Moreover, DC grids do not require bulky line-frequency transformers used in ac grids. It can be stated that DC grids can offer significant benefits, including higher efficiency, reduced complexity, lower costs, and the elimination of bulky transformers.

However, DC grids face several significant challenges that hinder their widespread adoption. One major obstacle is the lack of clear standardization, as there are no universally accepted voltage levels, interfaces, or protocols. This lack of standardization complicates the design and integration of different systems. Additionally, integrating DC grids with the existing AC-based infrastructure is a problematic, since most current power systems are built on AC technology. Furthermore, there is uncertainty in the market regarding the long-term viability and adoption of DC grids, which discourages investment and slows the development of necessary components and technologies. For these reasons, a universal converter suitable for both AC and DC grid applications is regarded as a potential solution. Fig. 1 illustrates the structure of the universal DC/DC-AC interface converter.

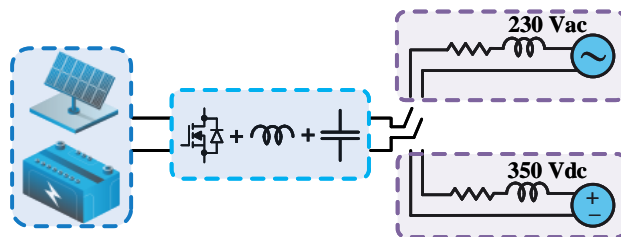


Fig. 1. Universal DC–DC/AC interface converter concept.

Most existing DC-AC inverters have the potential to function as universal DC-DC/AC power converters. In recent years, with the rising energy demand from RESs and battery storage systems, the topic of single-phase buck-boost capability in inverters has gained significant attention [13], [14], [15], [16], [17], [18], [19]. However, in these studies, each topology typically includes at least one capacitor, either connected to the DC bus or integrated within the main power circuit. These DC bus link capacitors or switched capacitors often have a large volume, which reduces the power density of the converter. Furthermore, capacitors generally exhibit a higher failure rate, indirectly affecting the overall lifespan of the system.

To address the aforementioned issues, this paper proposes a novel flying-inductor based dual-purpose DC/DC-AC interface converter. The proposed converter enhances efficiency, power density, and reliability by eliminating bulky DC-link

capacitors and reducing the number of inductors in the circuit. Additionally, it supports bidirectional operation, offers buck-boost capability, and includes reactive power control features, making it a versatile and robust solution. It can be further simplified to reduce the number of switches, making it suitable for applications requiring high power density.

The organization of this paper is as follows: Section II introduces the proposed converter. Section III details the operating modes of the proposed converter. Section IV discusses the system modeling and controller design. Section V outlines the design considerations for all key components within the converter. Section VI focuses on a comparative study between the proposed converter and previous designs. Experimental results are presented in Section VII. Finally, the advantages and limitations of the proposed converter are discussed in Section VIII.

II. PROPOSED FLYING-INDUCTOR BASED CONVERTER

Fig. 2 illustrates the proposed dual-purpose flying-inductor based converter. The proposed converter can operate in buck and buck-boost mode, allowing energy transfer from the input terminal to the output terminal across a wide input voltage range. This converter comprises nine switches (S_1 - S_9), one main inductor (L_1), two capacitors (C_f and C_s), and a solid state circuit breaker (SSCB). The SSCB ensures the system can shut down rapidly in the event of a fault, enhancing overall system safety.

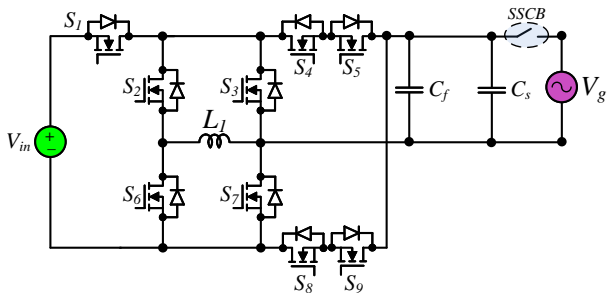


Fig. 2. Proposed FI-based single-phase buck-boost converter.

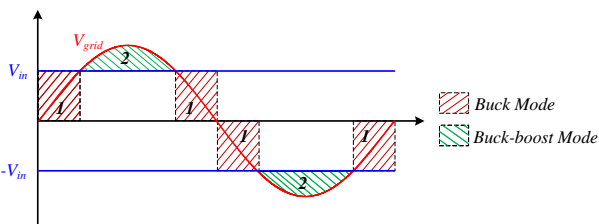


Fig. 3. Basic operation waveforms and operation mode at DC-AC state.

The proposed converter features a single charging inductor and eliminates the need for a bulky DC-link capacitor, thereby increasing its power density. Moreover, it can generate DC and AC voltages through the same output terminal, making it suitable for dual-purpose applications. Fig. 3 illustrates the basic operating principle of the proposed converter in DC-AC mode. The proposed converter has both buck and boost

capabilities over a wide input voltage range. When the input DC voltage (V_{in}) is higher than the peak grid voltage, the converter operates in buck mode, with only three switches (S_1 , S_2 , and S_6) in high-frequency switching mode. The converter can also operate in buck-boost mode at any input voltage level. In buck-boost mode, four switches operate in high-frequency switching mode during half of the cycle, while the remaining switches are either turned off or operate at the fundamental frequency. This modulation strategy ensures that the minimum number of switches operate in high-frequency mode during DC-AC conversion. Additionally, the converter supports bidirectional operation and includes advanced features such as reactive power control.

In certain applications, the proposed converter can be further simplified, as shown in Fig. 4, resulting in a reduced number of switches. However, the simplified version of the converter is limited to operating in buck-boost mode during the negative half-cycle.

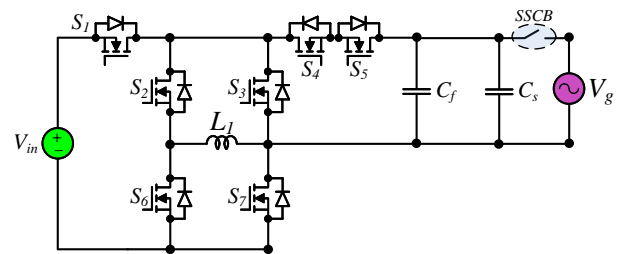


Fig. 4. Simplified proposed FI-based single-phase buck-boost converter.

III. OPERATION MODES OF THE PROPOSED TOPOLOGY

In this section, the performance of the proposed converter in DC-AC/DC-DC mode will be explained in detail.

The equivalent circuit along with the current path of DC-AC operation modes of the proposed converter are illustrated in Fig. 5. During the positive half cycle, when the instantaneous value of the output voltage is less than the input DC voltage, the proposed converter operates in positive buck mode, as shown in Fig. 5(a) and (b). In Fig. 5(a), the converter operates in the active state of buck mode, with switches S_1 , S_4 , S_5 , and S_6 in the ON state, allowing inductor L_1 to be charged from the input source. In Fig. 5(b), the converter operates in the freewheeling state of buck mode, with switches S_2 , S_4 , and S_5 in the ON state, enabling inductor L_1 to release energy to the output load. In positive buck mode, only switches S_1 , S_2 , and S_6 operate at the high switching frequency, while the remaining switches operate at the fundamental frequency or remain in the OFF state. This minimizes the switching losses of the proposed converter.

Fig. 5(b) and (c) illustrate the equivalent circuits of the proposed converter operating in buck-boost mode during the positive half-cycle. In this mode, the instantaneous output voltage exceeds the input DC voltage. Fig. 5(c) depicts the operation of the proposed converter in the active state of buck-boost mode. Switches S_1 , S_3 , S_4 , and S_6 are in the ON state, connecting inductor L_1 to the input voltage source, causing it

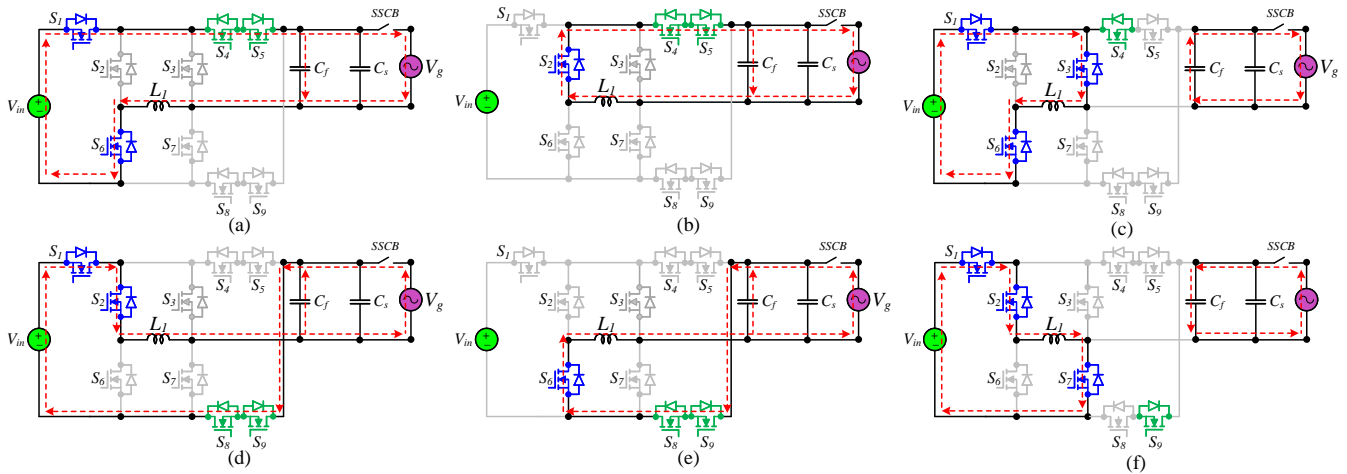


Fig. 5. Equivalent circuits of the proposed converter (blue switches operate at high-switching mode and green switches operate at ON state): (a) buck mode with active state during positive half cycle, (b) freewheeling state during positive half cycle for buck and buck-boost mode, (c) buck-boost mode with active state during positive half cycle, (d) buck mode with active state during negative half cycle, (e) freewheeling state during negative half cycle for buck and buck-boost mode, (f) buck-boost mode with active state during negative half cycle.

to enter charging mode. In Fig. 5(b), the proposed converter operates in the passive state of buck-boost mode. Switches S_2 , S_4 , and S_5 are in the ON state, allowing inductor L_1 to release stored energy to the grid.

Fig. 5(d) and (e) show the equivalent circuits and current paths for the buck mode during the negative half-cycle. In Fig. 5(d), the converter operates in the active state of buck mode during the negative half-cycle. In this mode, switches S_1 , S_2 , S_8 , and S_9 are in the ON state, transferring power from the input source to the output grid through inductor L_1 . In Fig. 5(e), the converter operates in the passive state of buck mode. Switches S_6 , S_8 , and S_9 are in the ON state, injecting the stored energy from inductor L_1 into the grid. During the negative buck operation, three switches operate at high switching frequencies, optimizing efficiency and minimizing switching losses.

The equivalent circuits of the proposed converter operating in buck-boost mode during the negative half-cycle are shown in Fig. 5(e) and (f). Fig. 5(f) illustrates the active state of buck-boost mode. In this state, switches S_1 , S_2 , S_7 , and S_9 are in the ON state, allowing inductor L_1 to be charged by the input source. The current passing through the capacitor C_f equals the output current. Fig. 5(e) depicts the passive state of buck-boost operation. In this state, switches S_6 , S_8 , and S_9 are in the ON state. During the buck-boost operation in the negative half cycle, switch S_9 remains fully ON, ensuring that the minimum number of switches operate at high switching frequency, thereby reducing switching losses.

The switching states for the proposed converter under transition mode are summarized in Table I.

IV. CONTROL ANALYSIS AND DESIGN

A. System Modeling

The proposed converter operates in either buck mode or buck-boost mode, depending on the instantaneous output voltage. To design an appropriate control structure, it is essential to model the system and analyze its behavior under

TABLE I
SWITCHING STATES FOR BUCK AND BUCK-BOOST MODE

	Positive half cycle		Negative half cycle	
	Buck	Buck-Boost	Buck	Buck-Boost
S_1	d_{buck}	$d_{\text{buckboost}}$	d_{buck}	$d_{\text{buckboost}}$
S_2	$1 - d_{\text{buck}}$	$1 - d_{\text{buckboost}}$	d_{buck}	$d_{\text{buckboost}}$
S_3	0	$d_{\text{buckboost}}$	0	0
S_4	1	1	0	0
S_5	1	$1 - d_{\text{buckboost}}$	0	0
S_6	d_{buck}	$d_{\text{buckboost}}$	$1 - d_{\text{buck}}$	$1 - d_{\text{buckboost}}$
S_7	0	0	0	$d_{\text{buckboost}}$
S_8	0	0	1	$1 - d_{\text{buckboost}}$
S_9	0	0	1	1

various operating conditions. The SSCB and capacitor C_s are primarily used to enable rapid system shutdown in the event of a fault. Since capacitor C_s has a small capacitance, it is not considered in the modeling analysis. In the buck-boost operation model, the modeling circuit of the proposed converter can be simplified as shown in Fig. 6. Based on Fig. 6, the state equations for the proposed converter operating in charging and discharging models can be described by (1) and (2), respectively.

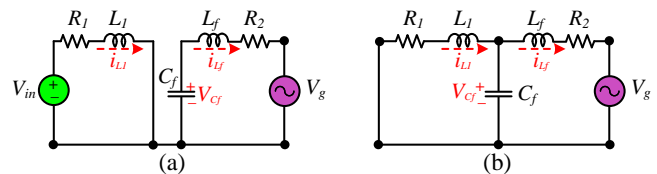


Fig. 6. Equivalent circuits during buck-boost operation with parasitic parameters: (a) charging mode, (b) discharging mode.

$$\begin{bmatrix} L_1 & 0 & 0 \\ 0 & C_f & 0 \\ 0 & 0 & L_f \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L1}(t) \\ V_{Cf}(t) \\ i_{Lf}(t) \end{bmatrix} = \begin{bmatrix} -R_1 & 0 & 0 \\ 0 & 0 & -1 \\ 0 & 1 & -R_2 \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ V_{Cf}(t) \\ i_{Lf}(t) \end{bmatrix} + \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_{in}(t) \\ 0 \\ V_g(t) \end{bmatrix} \quad (1)$$

$$\left. \frac{\hat{i}_{L_f}(s)}{\hat{d}(s)} \right|_{\substack{e_1(s)=0 \\ v_g(s)=0}} = \frac{V_{C_f}(1-D) - (R_1 + sL_1)I_{L1}}{s^3 L_1 L_f C_f + s^2 (L_1 C_f R_2 + L_f C_f R_1) + s(L_1 + L_f(1-D)^2 + C_f R_1 R_2) + R_1 + (1-D)^2 R_2} \quad (3)$$

$$\left. \frac{\hat{i}_{L_f}(s)}{\hat{d}(s)} \right|_{\substack{e_1(s)=0 \\ v_g(s)=0}} = \frac{V_{in}}{s^3 L_1 L_f C_f + s^2 (L_1 C_f R_2 + L_f C_f R_1) + s(L_1 + L_f + C_f R_1 R_2) + R_1 + R_2} \quad (4)$$

$$\begin{bmatrix} L_1 & 0 & 0 \\ 0 & C_f & 0 \\ 0 & 0 & L_f \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L1}(t) \\ V_{C_f}(t) \\ i_{L_f}(t) \end{bmatrix} = \begin{bmatrix} -R_1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -R_2 \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ V_{C_f}(t) \\ i_{L_f}(t) \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_{in}(t) \\ 0 \\ V_g(t) \end{bmatrix} \quad (2)$$

where R_1 and R_2 are the DC resistance of L_1 and L_f , respectively; $i_{L1}(t)$ and $i_{L_f}(t)$ are the currents through L_1 and L_f , respectively, and $V_{C_f}(t)$ is the voltage across the filter capacitor C_f .

The system model of the proposed converter can be further simplified using the average small signal modeling method, assuming that no perturbation in the input DC voltage or the output grid voltage. The transfer function between the inductor current $i_{L_f}(t)$ and duty cycle can be derived as (3). Given the small values of the parasitic resistances R_1 and R_2 , the system of the proposed converter can be approximated as a third-order system with one dominant pole, one high frequency conjugate pole, and one high frequency zero.

In buck operation mode, the system model of the proposed converter consists of a DC voltage source with an LCL filter connected to the grid. Since numerous studies have analyzed the small-signal model for this topology [20], [21], the transfer function between the inductor current $i_{L_f}(t)$ and the duty cycle is directly provided as (4).

B. Control Design

The system of the proposed converter is a typical third-order system, and its control strategy is represented in the block diagram shown in Fig. 7. In this study, several potential control strategies are evaluated for dual-purpose applications. Before the SSCB is connected, the control system identifies the type of the grid. If an AC grid is detected, the phase-locked loop (PLL) ensures system synchronization. The SSCB connects to the grid upon detecting a zero voltage crossing, allowing the system to operate properly with the AC grid-connected algorithm. If a DC voltage is identified, the snubber capacitor is precharged to match the output voltage level. The SSCB then turns on, initiating operation with the appropriate DC current control strategy. Under this control approach, the system can efficiently operate with both AC and DC grids without requiring additional computational resources.

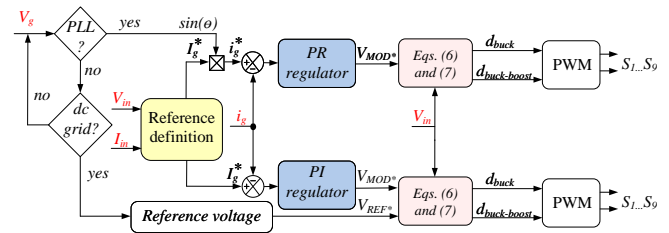


Fig. 7. Block diagram of the control system

The reference current (I_g^*) would be defined based on the specific applications. In the battery storage application, I_g^* is determined by the measured input voltage and current (V_{in} and I_{in}). In the PV application, I_g^* would be calculated using the maximum power point tracking (MPPT) algorithm. Once the amplitude of I_g^* is obtained, it is multiplied by the sinusoidal waveform from the PLL unit to produce the reference AC grid current (i_g^*). The error between the reference current (i_g^*) and the measured output current (i_g) is then fed into a Proportional and Resonant (PR) or Proportional Integral (PI) controller to generate the modulation voltage (V_{MOD}^*).

In the AC grid scenario, a PR controller is utilized in this study to achieve a high-quality output waveform. The PR controller enables precise control of AC signals by incorporating a resonant term that specifically targets the grid frequency. Furthermore, the PR controller can benefit from the suppression of the harmonic components in the current, which is essential for grid compliance and ensuring high power quality in inverter applications. However, in practical applications, the ideal PR controller faces challenges due to system delays, measurement errors, and stability concerns. To address these issues, a PR controller with a damping resonant filter is employed in this study, as shown in (5). By implementing a properly tuned PR controller, the system achieves stability and provides sufficient phase margin.

$$G_{PR}(s) = K_p + \frac{2Kr\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \quad (5)$$

where K_p is the proportional coefficient, Kr is the resonant coefficient, ω_c is the resonant bandwidth, and ω_0 is the resonant frequency, which is equal to $2\pi 50$ rad/s in this study.

In the DC grid scenario, appropriate current control is implemented to manage the switching operations, and a

conventional PI controller is employed to ensure stable and accurate performance.

V. CALCULATIONS OF THE INDUCTORS AND CAPACITORS

This section defines the passive components required for the proper operation of converter. Determining these values involves considering various operating modes.

The duty cycle for positive voltage generation in the buck operating mode is well known as:

$$d_{\text{buck}}(t) = \frac{v_{\text{out}}(t)}{V_{\text{in}}} \quad (6)$$

Considering the sinusoidal output waveform in the DC-AC mode, the AC value of the duty cycle in the buck operation mode can be calculated using (7).

$$d_{\text{buck}}(t) = \frac{V_{o,\text{max}} \cdot |\sin(\omega t)|}{V_{\text{in}}} \quad (7)$$

Similarly, the AC value of the duty cycle in the buck-boost operation mode can be calculated using (8) and the voltage gain can be calculated using (9).

$$d_{\text{b}_b}(t) = \frac{V_{o,\text{max}} \cdot |\sin(\omega t)|}{V_{\text{in}} + V_{o,\text{max}} \cdot |\sin(\omega t)|} \quad (8)$$

$$\frac{v_{\text{out}}}{V_{\text{IN}}} = \frac{d_{\text{b}_b}(t)}{1 - d_{\text{b}_b}(t)} \quad (9)$$

It should be noted that the maximum duty cycle $D_{\text{b}_b,\text{max}}$ during buck-boost operation occurs at the peak value of the output voltage and can be calculated using (10).

$$D_{\text{b}_b,\text{max}} = \frac{V_{o,\text{max}}}{V_{\text{IN}} + V_{o,\text{max}}} \quad (10)$$

To calculate the minimum value of L_1 , the worst case condition should be considered. Based on the control strategy, the inductor ripple reaches its maximum at the peak value of the grid voltage. Under this condition, the inductor current ripple can be calculated using (11).

$$\Delta i_L = \frac{V_{\text{in}} D_{\text{b}_b,\text{max}}}{L_1 f_{\text{sw}}} = K_{LL} \frac{I_{o,\text{max}}}{1 - D_{\text{b}_b,\text{max}}} \quad (11)$$

where V_{in} is the DC source voltage, $I_{o,\text{max}}$ is the peak value of the grid current, K_{LL} is the maximum percentage of the inductor current ripple, $D_{\text{b}_b,\text{max}}$ is the maximum duty cycle in buck-boost mode, and f_{sw} is the switching frequency. Based on the relationship between the average output power P_o and $I_{o,\text{max}}$, the value of L_1 can be calculated using (12).

$$L_1 = \frac{V_{\text{in}}^2 V_{o,\text{max}}^2}{2K_{LL} P_o f_{\text{sw}} (V_{\text{in}} + V_{o,\text{max}})^2} \quad (12)$$

where $V_{o,\text{max}}$ is the peak value of the grid voltage.

In order to calculate the value of the output capacitor filter C_f , the voltage integral equation for the filter capacitor must be formulated. The filter capacitor would have the maximum voltage ripple when the inductor current ripple is at its maximum. The calculation of the filter capacitor can be expressed using (13).

$$C_f = \frac{2P_o}{f_{\text{sw}} \Delta V_{C_f,\text{max}} (V_{\text{in}} + V_{o,\text{max}})} \quad (13)$$

VI. COMPARATIVE STUDY

In this section, in order to evaluate the advantages and disadvantages of the proposed converter, the performance of the design is compared with several other successful FI based converters [13], [17], [22], [23]. It should be noted that since each converter has been tested under different power levels and working conditions, it is difficult to directly compare their performance based on the information reported in previous research. To ensure a fair comparison, a few assumptions have been made in this study. First, the fundamental waveforms of the converter are determined by the basic modulation scheme, and their performance and characteristics are not directly influenced by specific design choices, such as switching frequency and selected semiconductors. This approach establishes general requirements for component sizing, including maintaining the same current ripple in the inductors and the same voltage ripple across the capacitors. Additionally, the volume of the inductors and capacitors is estimated based on their maximum stored energy, as calculated using (14) and (15).

$$W_L = 0.5 \times \sum_{i=1}^{N_L} L_i \cdot I_{L,\text{max}}^2 \quad (14)$$

$$W_C = 0.5 \times \sum_{i=1}^{N_C} C_i \cdot V_{C,\text{max}}^2 \quad (15)$$

where L_i and C_i are the values of the i th inductance and capacitance; N_L and N_C are the number of inductors and capacitors, respectively; $I_{L,\text{max}}$ is the peak value of inductor current, and $V_{C,\text{max}}$ is the peak capacitor voltage.

The internal resistance for the inductor with a value of 500 μH is considered to 75 $\text{m}\Omega$, and the internal resistance of inductors with other value can be calculated using (16).

$$R_{L,\text{new}} = \sqrt{\frac{L_{\text{new}}}{L_{\text{base}}}} R_{L,\text{base}} \quad (16)$$

In addition, the conduction losses in power switches can be calculated using (17). Conduction losses of the inductors and capacitors can be obtained from (18) and (19), respectively.

$$P_{\text{con},S} = R_{ds,\text{on}} \cdot I_{\text{rms},S}^2 \quad (17)$$

$$P_{\text{con},L} = \text{ESR}_L \times I_{\text{rms},L}^2 \quad (18)$$

$$P_{\text{con},C} = \text{ESR}_C \times I_{\text{rms},C}^2 \quad (19)$$

where $I_{\text{rms},S}$ is the rms current of switch, $R_{ds,\text{on}}$ is the internal resistance of power switch, $I_{\text{rms},L}$ is the rms current of the inductor, ESR_L is the equal series resistance of the inductor, $I_{\text{rms},C}$ is the rms current of the capacitor, and ESR_C is the equal series resistance of the capacitor.

The switching losses are defined in (20), where V , I , t_{ON} , t_{OFF} , and f_{sw} represent the voltage stress over the switch in the turn-off state, current stress of the switch in the turn-on state, turn-on time, turn-off time, and switching frequency, respectively.

$$P_{\text{sw},S} = \frac{1}{6} \times V \times I \times (t_{\text{ON}} + t_{\text{OFF}}) \times f_{\text{sw}} \quad (20)$$

Moreover, the total standing voltage (TSV) across the all switches is considered as one of the criteria in this comparative

study to indicate the overall cost of the required semiconductors. The TVS can be calculated using (21).

$$\text{TSV} \approx \sum_{i=1}^{N_S} \frac{\hat{v}_{Si}}{V_{in}} \quad (21)$$

where \hat{v}_S is the maximum voltage stress across the semiconductors.

TABLE II
SIMULATED PARAMETERS OF PROPOSED CONVERTER

Parameter	Value
Input voltage (V_{IN})	200 V
Output voltage peak value ($V_{o,max}$)	330 V
Switching frequency (f_{sw})	30 kHz
Output power (P_p)	1000 W
On-state resistance of power switch ($R_{ds,on}$)	50 m Ω
Forward voltage of the power diode (V_{fw})	0.7 V
On-state resistance of power diode ($R_{d,on}$)	50 m Ω
Internal resistance of 500 μ H inductor ($R_{L,base}$)	75 m Ω
Current ripple of main inductor (Δi_L)	30%
Voltage ripple across capacitor (ΔC_V)	5%
Current ripple of the output filter inductor	5%

Table II describes the simulated parameters of the proposed converter. To ensure a fair comparison under identical operating conditions, the input voltage, output voltage, switching frequency, and output power are maintained consistently across all structures.

Table III illustrates the comparison chart between the proposed converter with other topologies. It includes the number of switch devices, the number of passive components, stored energy inside the inductors W_L , stored energy inside the capacitors W_C , boosting factor, conduction losses P_{con} , switching losses P_{sw} , TSV, total current standing (TCS), and output power P_o .

The proposed converter exhibits the lowest stored energy in inductors and capacitors among the compared topologies. This is primarily because it does not require bulky DC-link capacitors and uses fewer inductors in the circuit. The converters in [17], [22] have higher stored energy in the capacitors due to the presence of one or two large DC-link capacitors. Meanwhile, the converters in [13], [23] have higher total stored energy in both inductors and capacitors, as they incorporate more passive components to facilitate energy transfer and waveform filter. The lowest stored energy in passive components also indicates that the proposed converter has the advantages in terms of high power density.

In terms of losses, the proposed converter exhibits the lowest conduction losses. Although the converters in [13], [22] use fewer switching devices than the proposed converter, converter [13] includes two additional inductors and two more capacitors, while converter [22] has two more inductors. The conduction losses of converters [17], [23] are higher than those of the proposed converter due to the more number of switching devices and passive components. Converters in [13], [17], [22] have lower switching losses because they use fewer switching devices and have lower total voltage stress (TVS). In contrast, the converter in [23] has higher switching

losses than the proposed converter due to its larger number of switching devices and higher TVS. Regarding TVS and TCS, the converters in [13], [17], [22] exhibit better performance than the proposed converter. However, the converter in [23] has higher TVS and TCS values due to its larger number of switching devices.

In conclusion, it should be acknowledged that the proposed converter does not outperform all compared solutions in all parameters. However, its overall figure of merit is highly competitive. Obviously, the proposed converter demonstrates significant strengths in terms of efficiency and the reduced size of passive components, making it a promising option for industrial applications.

VII. EXPERIMENTAL RESULTS

The experiment section is devoted to evaluating the performance and features of the proposed inverter. To verify the performance and operation of the proposed FI-based converter, some experimental results are provided. Fig. 8 shows a picture of the experimental prototype. Table IV describes the parameters of the proposed universal converter. To produce the PWM signals for the switches and control the operations of the proposed converter, the TSM320F280049 microcontroller was used. The control circuit was supplied with a 12 V input voltage provided by the NSP-3630 Manson power supply. The power circuit was realized using a four-layer PCB, which includes the power switches, the charging inductor, the capacitor, the input filter, and the output filter. A common heatsink was used to balance the temperature of the power switches. All measurement results were obtained using Tektronix TPA-BNC voltage probes, Tektronix TCP0150 current probes, and a Tektronix MDO4034B-3 digital oscilloscope. The YOKOGAWA WT1806E power analyzer was used to measure efficiency. The input voltage was supplied by a programmable DC power supply, the Chroma 62150H-1000s. The experimental tests aim to achieve three main goals: firstly, to evaluate the performance of the proposed converter under DC-AC and DC-DC modes; secondly, to test the feasibility of buck-boost and buck operations in each mode; and thirdly, to analyze the efficiency and losses of the proposed converter. In DC-AC mode and DC-DC mode, nominal peak output voltages of 330 Vac and 350 VDC, respectively, were considered. It should be noted that only one film capacitor was used as part of the output filter. The electrolytic capacitor and the middle film capacitor serve as decoupling capacitors, connected in parallel with the DC supply, or to implement passive decoupling if low-frequency decoupling is required. This makes the input power constant.

Fig. 9 shows the performance of the proposed dual-purpose DC-AC/DC-DC converter in DC-AC mode. Fig. 9 (a) illustrates the output voltage after filtering (V_{out}), the output current after filtering (I_{out}), the input voltage (V_{in}), and the flying-inductor current (I_L). The input voltage is 400 V and the output voltage is a sinusoidal waveform with a maximum value of 330 V. Therefore, the proposed converter operates in the buck mode at the output power of 1.5 kW. In this figure, I_{out} is a sinusoidal 50 Hz waveform and its peak value equals

TABLE III
COMPARISON TABLE BETWEEN PROPOSED CONVERTER AND OTHER CONVERTERS

Ref.	N_s	N_D	N_L	N_C	W_L (mJ)	W_C (J)	TVS (p.u.)	TCS	Gain	P_{con} (W)	P_{sw} (W)	Effi. (%)	P_o (kW)
[13]	6	–	3	3	201.5	0.636	11.9	$2i_{L1m} + 4i_{L2m}$	$\frac{d}{1-d}$	28.1	8.29	96.4	1
[17]	6	4	3	3	302.9	108.5	11.9	$10i_{Lm}$	$\frac{0.5}{1-d}$	72.3	8.73	92.5	1
[22]	6	1	2	2	158.4	11.2	11.9	$7i_{Lm}$	$\frac{d}{1-d}$	21.8	5.07	97.4	1
[23]	11	0	3	1	183	0.546	17.2	$13i_{Lm}$	$\frac{2d}{1-d}$	31.7	14.77	95.6	1
Proposed	9	–	1	1	147.7	0.408	15.85	$9i_{Lm}$	$\frac{d}{1-d}$	16.2	10.52	97.4	1

TABLE IV
PARAMETERS OF THE PROPOSED UNIVERSAL CONVERTER

Parameter	Value
Peak value of grid voltage ($V_{o,max}$)	330 VAC / 350 VDC
Maximum output power (P_p)	2500 (DC-AC)/5000 (DC-DC) W
Input voltage range	100-400 V
Flying inductor (L_1)	0.35 mH
Output filter capacitor (C_f)	3.3 μ F
Decoupling capacitor (C_1)	3.3 μ F
Switches ($S_1 \sim S_9$)	FMG50AQ120N

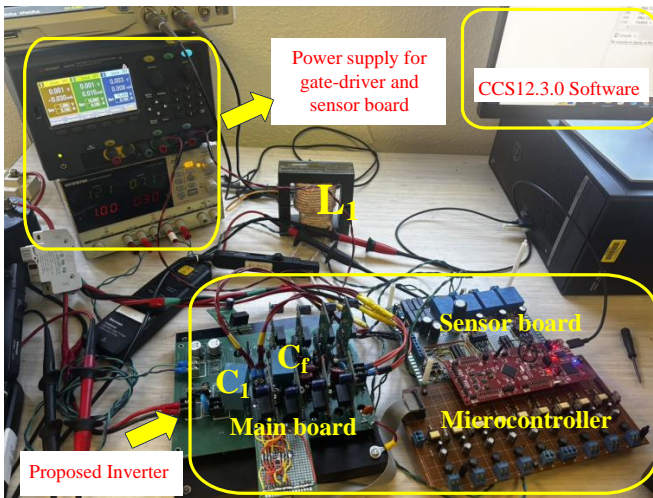


Fig. 8. Photo of the experimental prototype (2.5 kW/ 5 kW) of the proposed converter.

to approximately 10 A. It is also in phase with V_{out} under purely resistive load. The total harmonic distortion (THD) values of the output voltage and output current are 1.9% and 1.9%, respectively, as measured by the YOKOGAWA power analyzer. The power factor (PF) value is equal to 1. Fig. 9 (b) shows the experimental results under $P_{out}=1.6$ kW and $V_{in} = 200$ V test conditions for buck-boost mode. The output voltage still achieve the purely sinusoidal waveform with the peak of 330 V. I_{out} has the same phase with the output voltage under purely resistive load. Since the input voltage is lower in this case, the more current would be injected into the inductor. The peak value of the inductor current can be up to 25 A. THD values of the output voltage and output current are 0.9% and 0.866%, respectively, as measured by the YOKOGAWA power analyzer. The PF value is equal to 1. Fig. 9 (c) shows the experimental results under test conditions of $P_{out}=1.6$

kW and $V_{in} = 200$ V for buck and buck-boost modes. The output voltage has the purely sinusoidal waveform and peak value is up to 330 V. The output voltage exhibits a purely sinusoidal waveform with a peak value of up to 330 V. The inductor current shows a smooth transition during the mode change between buck and buck-boost operation. The efficiency during the transient mode is 95.682%, primarily limited by the increased inductor ripple in the buck-boost mode. The THD values of the output voltage and current are 2% and 1.97%, respectively, as measured by the YOKOGAWA power analyzer. The PF value is equal to 1.

Fig. 10 shows the step change and reactive power control of the proposed converter under DC-AC mode. Fig. 10 (a) and (b) show the dynamic evaluation of the proposed converter in the DC-AC mode. In Fig.10 (a), a step change in output power from 1.5 kW to 2.5 kW is occurred. The increase in load power causes both the output current and the flying inductor current to rise, balancing the power demand. The output voltage maintains its sinusoidal waveform throughout. Similarly, Fig.10 (b) illustrates a step change from 2.5 kW to 1.5 kW, where both the output current and the flying inductor current decrease in response to the reduced output power. Fig. 10 (c) shows the performance of the proposed converter under the nonunity power factor.

Fig. 11 illustrates the operation of the proposed dual-purpose DC-DC/DC-AC power converter under DC-DC mode. In all DC-DC modes, the output voltage is equal to 350 V. Similar to DC-AC experimental tests, two input voltages were considered as $V_{in} = 200$ V, $V_{in} = 400$ V to validate the buck and buck-boost capability of the proposed solution, respectively. The results in Fig. 11(a) were recorded when P_{out} was 5 kW and V_{in} was set to 400 V. It is seen that V_{out} equals 350 V, which confirms that the proposed solution steps down the voltage successfully. Fig. 11(b) illustrates the results when P_{out} was 3.2 kW and V_{in} was 400 V. In this figure, the converter operates in the buck-boost mode, the flying inductor current would have the higher current ripple and peak current in this operation. Fig. 11(c) illustrates the results when P_{out} was 2 kW and V_{in} was 200 V. The output voltage was regulated to 350 V, which proves that the proposed converter can operate in buck-boost mode successfully.

Fig. 12 shows the voltage stress across all MOSFETs. In this study, the input voltage is set to 400 V, and the peak output voltage is 330 V. Fig. 12(a) shows the voltage stress of switches S_1 , S_2 , and S_6 . It should be noted that the voltage across S_1 , V_{ds1} , is almost zero during the positive half cycle. When the converter operates in freewheeling mode, the body

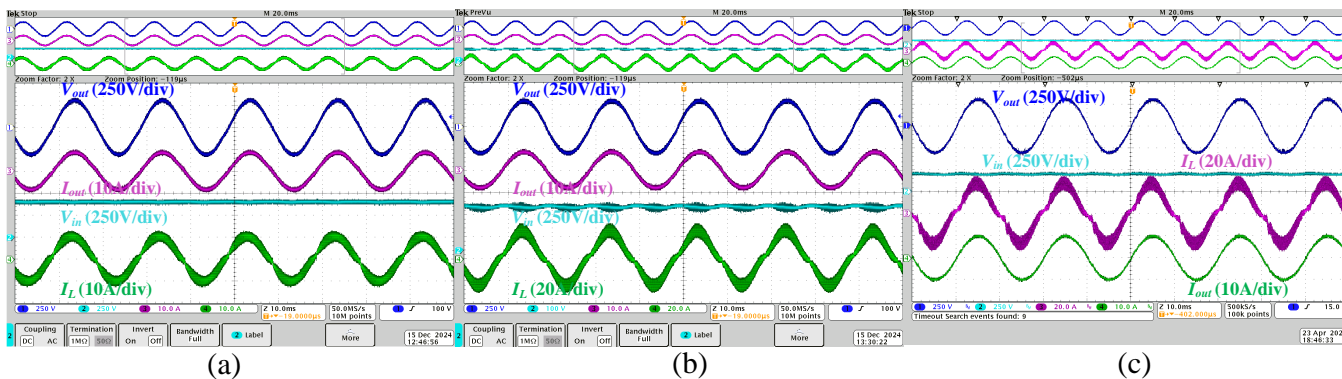


Fig. 9. Steady-state experimental results in the DC-AC mode: the output voltage, the output current, the input voltage, and the current of flying inductor. (a) the output power at 1.5 kW and 400 V input voltage under buck mode. (b) the output power at 1.64 kW and 200 V input voltage under buck-boost mode. (c) the output power at 1.63 kW and 200 V input voltage under buck and buck-boost mode.

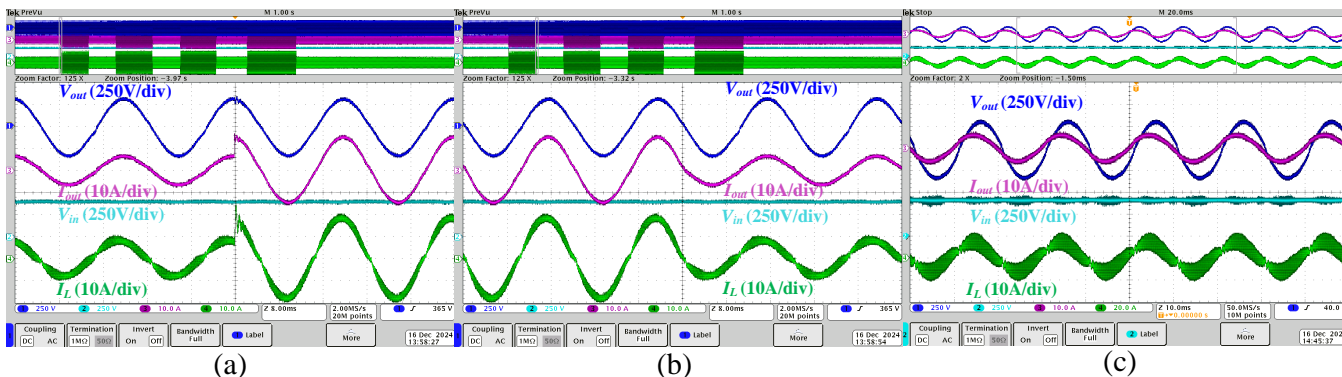


Fig. 10. Experimental results in the DC-AC mode: the output voltage, the output current, the input voltage, and the current of flying inductor. (a) a step change at the output power from 1.5 to 2.5 kW under buck mode. (b) a step change at the output power from 2.5 to 1.5 kW under buck mode. (c) Leading power factor.

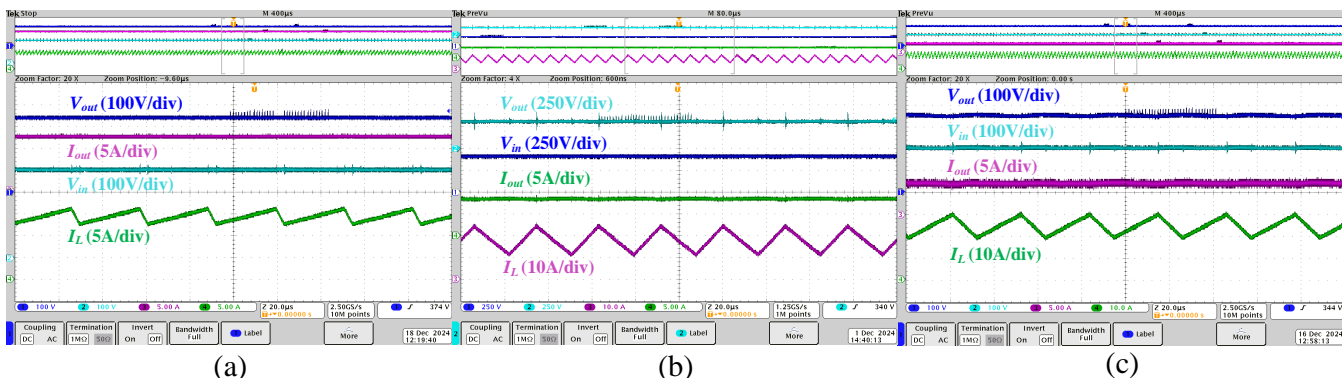


Fig. 11. Experimental results in the DC-DC mode: the output voltage, the output current, the input voltage, and the current of flying inductor. (a) the output power at 5 kW and 400 V input voltage under buck mode. (b) the output power at 3.2 kW and 400 V input voltage under buck-boost mode. (c) the output power at 2 kW and 200 V input voltage under buck-boost mode.

diode of S_1 is forced to turn on, and the voltage across S_1 is equal to the voltage drop of the diode. In this case, the voltage stress of S_2 and S_6 are equal to the input voltage. Fig. 12(b) shows the voltage stress of switches S_3 , S_4 , and S_5 . The voltage stress of S_3 is equal to the input voltage, and voltage stress of S_5 is equal to output voltage. Fig. 12(c) shows the voltage stress of switches S_7 , S_8 , and S_9 .

Fig. 13 illustrates the experimental efficiency curves of the

proposed converter in different operation modes. Fig. 13(a) shows the efficiency curve of the converter in DC-AC mode. The output power was extended up to 2.85 kW. The converter was tested under three different operating conditions, with an output voltage peak of 330 V. The input voltage was 400 V in buck operation and 200 V in both buck-boost and hybrid buck + buck-boost operations. As can be seen, during buck operation, the proposed converter achieves the highest

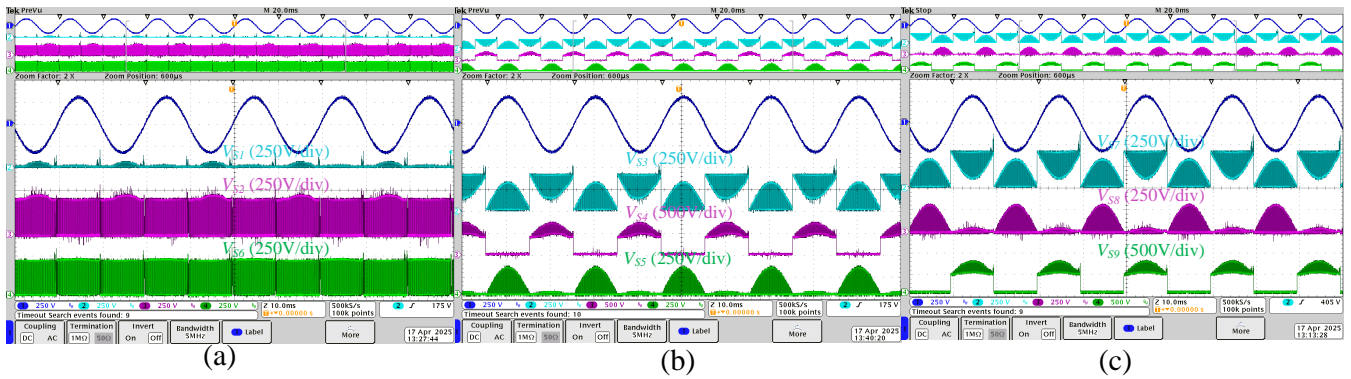


Fig. 12. Experimental results of the voltage stress across each MOSFET. (a) voltage stress of S_1 , S_2 , and S_6 . (b) voltage stress of S_3 , S_4 , and S_5 . (c) voltage stress of S_7 , S_8 , and S_9 .

efficiency, reaching up to 98.07% at 0.9 kW. The buck-boost operation exhibits relatively lower efficiency than the other operation due to higher inductor current ripple. The hybrid buck + buck-boost operation demonstrate better performance than the buck-boost operation, achieving an efficiency of up to 97.56% at 0.8 kW. Fig. 13(b) shows the efficiency curve of the converter in DC-DC mode. The output power was extended up to 6.6 kW. The converter was tested under two different operating conditions, with a DC output voltage of 350 V. The efficiency reaches nearly 99.2% at 2.18 kW during the buck operation, when the input voltage is equal to 400V. The maximum efficiency achieved is 98.45% in buck-boost operation the input voltage of 200V.

VIII. CONCLUSION

This paper presents a dual-purpose DC-DC/DC-AC power converter based on a flying-inductor topology. The proposed solution leverages the unique characteristics of the flying inductor to achieve a wide input voltage range and high efficiency while reducing the number of inductors and capacitors required. Due to the minimization of passive component, wide input voltage range, and buck-boost ability, this topology is an excellent candidate for dual-purpose applications involving both DC and AC grids.

The laboratory prototype was developed to validate the operation of the proposed inverter, achieving a power rating of 2.5 kW in the DC-AC mode and 5 kW in the DC-DC mode. Comprehensive analysis of all operating modes and associated switching states was conducted. A closed-loop control strategy based on a proportional-resonant (PR) controller was applied in grid-off scenarios.

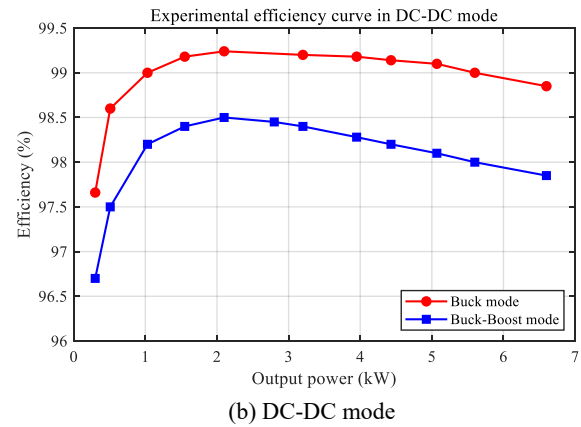
The peak efficiency of the system reached 98% in DC-AC mode and nearly 99% in DC-DC mode, demonstrating the superior performance of the flying-inductor-based converter. Additionally, a comparison with existing topologies highlighted the advantages of the proposed solution, including its simplified design and enhanced performance metrics. The results underscore that this flying-inductor-based inverter is a highly promising candidate for industrial applications.

IX. ACKNOWLEDGMENT

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(a) DC-AC mode



(b) DC-DC mode

Fig. 13. Experimental efficiency study: efficiency of the proposed converter under different operating modes. (a) DC-AC mode, (b) DC-DC mode.

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X. REFERENCES SECTION

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XI. BIOGRAPHY SECTION

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