
A control method to improve the efficiency of a soft-switching non-isolated bidirectional DC-DC converter for hybrid and plug-in electric vehicle applications

Lei Jiang

National Engineering Laboratory for Automotive
Electronic Control Technology,
Shanghai Jiao Tong University,
Shanghai, China

and

Department of Electrical and Computer Engineering,
University of Michigan – Dearborn,
Dearborn, Michigan, USA
Email: Lei_Jiang@126.com

Chris Mi*

Department of Electrical and Computer Engineering,
University of Michigan – Dearborn,
Dearborn, Michigan, USA
Email: chrismi@umich.edu

*Corresponding author

Siqi Li

Department of Electrical Engineering,
Kunming University of Science and Technology,
Kunming 650500, Yunnan, China
Email: lisiqi00@gmail.com

Chengliang Yin

National Engineering Laboratory for Automotive
Electronic Control Technology,
Shanghai Jiao Tong University,
Shanghai, China
Email: clyin1965@sjtu.edu.cn

Abstract: Hybrid energy storage system (HESS) can be adopted in hybrid, plug-in hybrid, and pure electric vehicles (HEV, PHEV, and EV), where a bidirectional DC-DC converter (BDC) is used to connect batteries and ultra-capacitors. The efficiency improvement of the BDC is beneficial to increase the efficiency viability of HESS. Due to ZVS, high efficiency can be obtained at heavy load operations while the efficiency is low at light load operations mainly because of the conduction losses of the auxiliary circuits. These losses

can be reduced by optimising the switching frequency. The relationship of efficiency and switching frequency are presented and discussed. A scaled-down 1 kW BDC prototype is built to verify the feasibility of the efficiency improvement. With the aim of achieving ZVS conditions and variable frequency control, the implementing method is proposed. The simulated results are also presented, which can validate the feasibility of the proposed control method.

Keywords: maximum efficiency; HESS; hybrid energy storage system; DC-DC power conversion; resonant power conversion; variable frequency control; peak-valley control; DC-DC converter; zero voltage switching; bidirectional.

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Biographical notes: Lei Jiang received the BS and MS from Sichuan University, Chengdu, China, in 2006 and 2009, respectively. Since 2009, he has been working toward the PhD degree in the National Engineering Laboratory for Automotive Electronic Control Technology at Shanghai Jiao Tong University, Shanghai, China, and his major is the Automotive Engineering. During 2011–2012, he was a joint PhD student with the DOE GATE Center for Electric Drive Transportation in University of Michigan, Dearborn. His research interests include soft-switching technologies of dc-dc converters, hybrid energy storage systems (HESS), vehicle controllers, battery management systems (BMS), and on-board chargers.

Chris Mi is Professor of Electrical and Computer Engineering, and Director of the newly established DOE funded GATE Center for Electric Drive Transportation at the University of Michigan – Dearborn. Previously he was an Electrical Engineer with General Electric Canada Inc. He received the BS and MS degrees from Northwestern Polytechnical University, Xi'an, China, and the PhD degree from the University of Toronto, Canada, all in Electrical Engineering. His research interests include electric drives, power electronics, electric machines; renewable energy systems; electrical and hybrid vehicles.

Siqi Li received the BS and PhD degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 2004 and 2010, respectively. He is now a Lecturer with the Department of Electrical Engineering, Kunming University of Science and Technology. He was a Postdoctoral Fellow with the Department of Electrical and Computer Engineering, University of Michigan, Dearborn from 2011 to 2013. His research interest focuses on battery management system and high performance battery charger for electric vehicles.

Chengliang Yin received the MS and PhD degrees in Vehicle Engineering from Jilin Industrial University, Changchun, China, in 1996 and 2000, respectively. He is currently a Professor with Shanghai Jiao Tong University, where he is also the Vice Dean of Institute of Automotive Engineering as well as the Vice Director of National Engineering Laboratory for Automotive Electronic Control Technology. His research interests include the control of automotive electronics, electric vehicles, especially the research and development of hybrid electric vehicles.

1 Introduction

Hybrid, plug-in hybrid and pure electric vehicles (HEV, PHEV, and EV) are as a good choice for many countries to reduce emissions, reduce oil dependency, increase energy security and protect the environment. The batteries, as an on-board energy storage system, are critical for the performances of the vehicles, such as mileages, accelerating performance, and so on. Due to the low power density of currently available batteries, a Hybrid Energy Storage System (HESS) is developed to mitigate the above-mentioned problems. A HESS is composed of a high-energy density component such as battery and a high-power density component such as ultra-capacitor. There are many topologies of HESS, and BDC is a very significant component in HESS which can transfer energy between the battery, the ultra-capacitor and the motor inverter with any needed direction and magnitude (Lajunen and Suomela, 2012; Zandi et al., 2011; Shuai et al., 2007; Zhang and Jiang, 2012; Bai and Mi, 2012; Marco and Vaughan, 2012; Wang et al., 2013; Bai et al., 2010; Cao and Emadi, 2012). The efficiency improvement of BDC is critical to reduce the energy losses when transferring power between multiple energy systems, so more energy can be used to drive the vehicles (Bai and Mi, 2008). This paper mainly focuses on non-isolated BDC used for HESS, which usually utilise a combination of a buck converter and a backwards boost converter. These converters only operate at a buck or boost mode at any given time, so the operating characteristics are the same as those of buck and boost converters. Such converter are typically rated about 10–100 kW for EV and PHEV applications. Due to the limitations of our laboratory, only a scaled-down prototype of 1 KW was built to validate the proposed method. We believe the principle will also apply to real world application at the higher power level.

In order to realise high efficiencies of DC-DC converters, soft-switching technologies are adopted, including Zero-Voltage-Switching (ZVS) and zero-current-switching (ZCS). ZVS is the most common soft-switching technology, where the anti-parallel body diode conducts before the semiconductor switch is turned on.

In many previous papers (Das et al., 2009; Chau et al., 1998; Aamir and Kim, 2011), adding auxiliary switches, inductors and capacitors is used to achieve ZVS and ZCS conditions, but high voltage and current stresses of power switches are also generated. Zhang et al. (2007) and Ni et al. (2010) adopted interleaved structures to achieve ZVS conditions. Usually, several conventional synchronous DC-DC converters are connected in parallel. However, there are many components like semiconductor switches and inductors, which will result in high cost and complex control schemes. Another important method is to utilise coupled inductor by adding a winding with the main inductor, which can supply another power flow channel to make the inductor current flow through zero (Do, 2011; Zhang and Sen, 2003). The proposed ZVS non-isolated BDC improved from the coupled inductor topology can be considered as a solution of soft-switching topology of BDC in HESS (Zhang and Sen, 2003).

Due to soft-switching, the switching losses are approximately equal to zero so the conduction losses are dominant in the overall power losses. However, the recycled power will be also generated in this topology, which is not beneficial for efficiency improvements. Compared with conventional buck and boost converters, higher efficiencies can be obtained at heavy load conditions, but the efficiency at light load conditions is lower because of the additional conduction losses of the auxiliary circuits, which are necessary

to achieve ZVS conditions. Therefore, how to improve the efficiency at light load conditions based on soft-switching Bidirectional DC-DC Converters (BDC) is important, but there is a lack of research in this area up to now.

In order to improve efficiencies, the parameter optimisations of the hardware like inductors and capacitors are necessary, but they are usually done for a specific load and will not result in maximum efficiencies at another load condition. Also, the hardware parameters are not able to be adjusted once circuit is in operation. Hence, the only parameter to be optimised for power converters is the switching frequency. As for conventional hard-switching buck or boost converters, there are many studies about improving efficiencies at light load conditions (Arbetter et al., 1995; Gildersleeve et al., 2002; Wang et al., 1997; Yu and Lai, 2008; Pahlevaninezhad et al., 2012), and some of them are useful for soft-switching converters as well. Usually, variable switching frequency schemes have been utilised at light load conditions in conjunction with Discontinuous Conduction Mode (DCM) to improve efficiencies. In the work of Arbetter et al. (1995), the synchronous buck converter always operates in the DCM, which is implemented by adjusting the switching frequency. The lower MOSFET is turned off when the inductor current is zero, and the switching losses can be reduced. Operating in DCM at light loads prevents the inductor current from going negative, and there is no recycled energy in the synchronous converter, so the conduction losses will be reduced. Moreover, DCM is with a lower frequency compared to CCM, which is beneficial to improve efficiencies. A larger filter capacitor is needed to smooth the large current ripple. The dynamic and steady-state performances are also impacted because there are oscillations when the inductor current is zero. To solve this problem, Gildersleeve et al. (2002) and Wang et al. (1997) proposed a mode-hopping technique (MH), and the converters operate in synchronous mode at a Continuous Conduction Mode (CCM) at medium to heavy load conditions, and the inductor current remains positive. When the load is light, it will operate at DCM, where the low synchronous rectifier is always off. In the work of Pahlevaninezhad et al. (2012), the frequency of the modulator is adjusted based on the converter load, and a simple lookup table is adopted to adjust the frequency accordingly. We believe that this topology is very suitable for HESS applications but the efficiency needs further optimisation.

In the soft-switching DC-DC converters, the soft-switching conditions and the variable frequency control should be achieved simultaneously at all load conditions. However, different soft-switching topologies have different constraints for achieving soft-switching conditions, and the optimal switching frequency is also different. It is hard to develop a uniform control method for all soft-switching converters, but for similar soft-switching topologies, a common control method is likely to be derived.

In this paper, based on the proposed BDC, the relationship analyses of efficiencies, switching frequencies and output power are presented and discussed. The measured efficiencies at several fixed switching frequencies are presented to validate the theoretical analyses. It is showing that increasing the switching frequency can improve efficiency at light load conditions. Furthermore, there is a trade-off between switching frequency and soft-switching conditions. Hence an innovative peak-valley control method is proposed to realise the trade-off. Both the peak and valley values of the inductor current are controlled. In buck mode, the valley values are controlled for implementing ZVS conditions while the peak value is controlled for adjusting the output objective (voltage

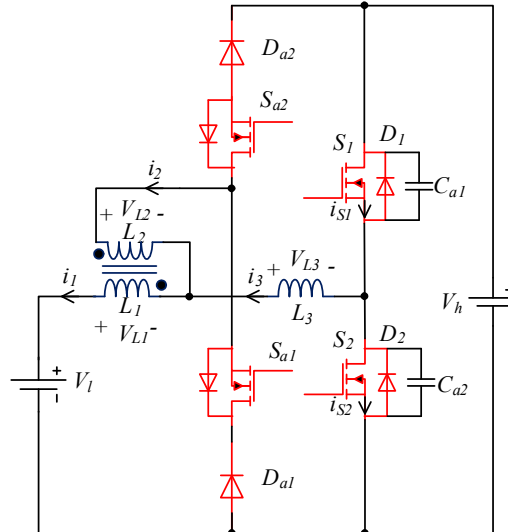
or current). In boost mode, the function is similar but the swapping of peak and valley values is needed. The simulated results of this new method are also given, which can clearly demonstrate the control effects.

2 Converter topology and efficiency analyses

2.1 Introduction to the proposed ZVS converter

The proposed ZVS BDC topology, as shown in Figure 1, consists of an coupled inductor (L_2), the main inductor (L_1), a small inductor (L_3), two auxiliary MOSFETs (S_{a1}, S_{a2}), two auxiliary diodes (D_{a1}, D_{a2}), as well as two main MOSFETs (S_1, S_2). The main MOSFETs (S_1, S_2) can operate under ZVS conditions at all load conditions while the auxiliary MOSFETs and diodes (S_{a1}, S_{a2}, D_{a1} and D_{a2}) work under ZCS conditions. S_{a1} and S_{a2} , operating like relays, are used to switch the mode between buck mode and boost mode. S_{a2} is always off and S_{a1} is always on in buck mode, and S_{a1} is always off and S_{a2} is always on in boost mode. For this converter, the operating principles of the buck mode and the boost mode are similar. The characteristics of the waveforms of i_1, i_2 and i_3 are similar, and only the directions are opposite. Therefore, it can be considered that the efficiency characteristics of the buck mode and the boost mode are similar, so only the efficiency analyses and experimental verifications in buck mode are presented in this paper. The drawn conclusions are also suitable for boost mode.

Figure 1 The proposed ZVS bidirectional DC/DC topology (see online version for colours)

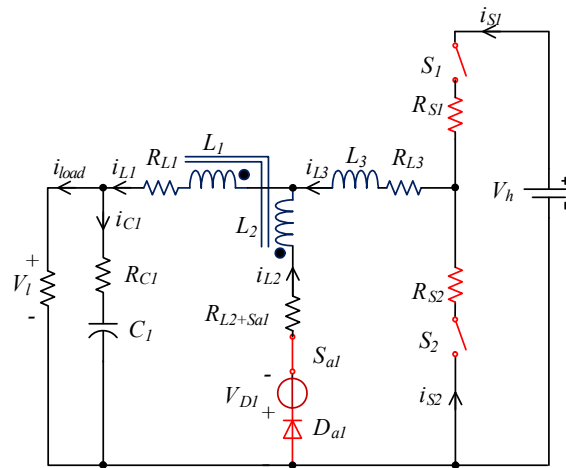


2.2 Theoretical analyses

All the following analyses are based on that the converter operates at a steady-state condition. For efficiency analyses, some simplifications and assumptions are also needed. Due to soft-switching abilities, switching losses in this converter are not considered, so

the conduction losses are the dominate power losses. The conduction losses are a result of MOSFET parasitic resistances R_{DS-ON} , the inductors DCR (including the traces resistances), and the forward voltage drop of diodes. Also, they are a function of the load current and switching frequency. The simplified equivalent schematic of the proposed converter in buck mode is shown in Figure 2, where the parasitic resistances of each component such as S_1 , S_2 , R_{L1} , R_{L2+Sa1} , R_{L3} and R_{C1} are shown, and D_1 is equivalent to an ideal diode and a voltage source (forward voltage) V_{D1} .

Figure 2 The equivalent schematic of the proposed converter in buck mode (see online version for colours)



The operating in one switching circle is simplified to three modes because the switching processes are neglected for the soft-switching converter while analysing efficiencies. Also, the simplified equivalent circuits of each mode are shown in Figure 3.

Figure 3 Equivalent circuits for each operation mode of buck mode. (a) Mode 1, t_0-t_1 ; (b) Mode 2, t_1-t_2 ; (c) Mode 3, t_2-t_3 (see online version for colours)

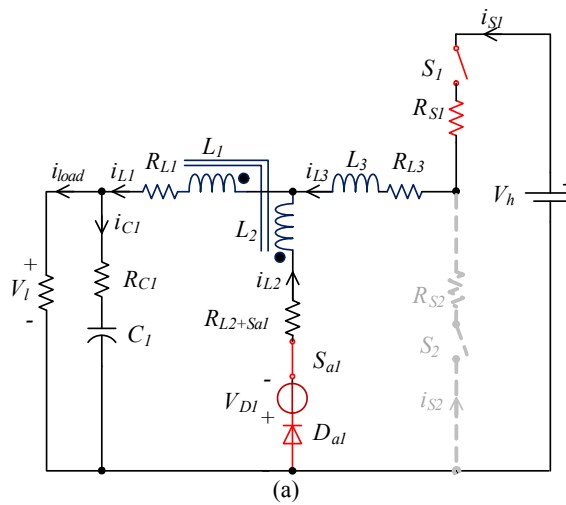
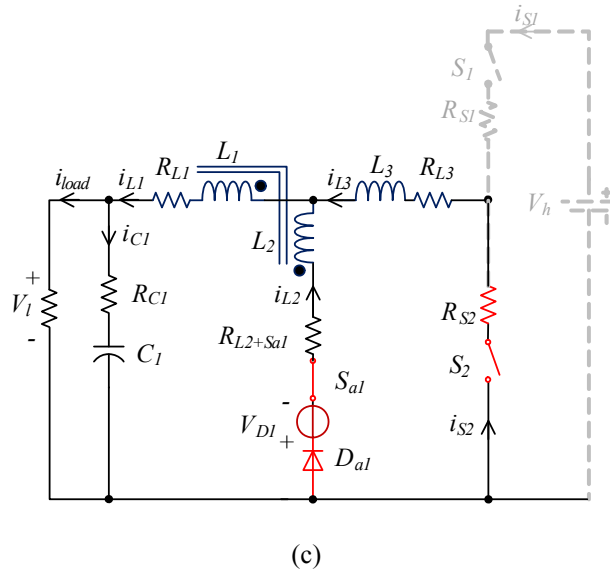
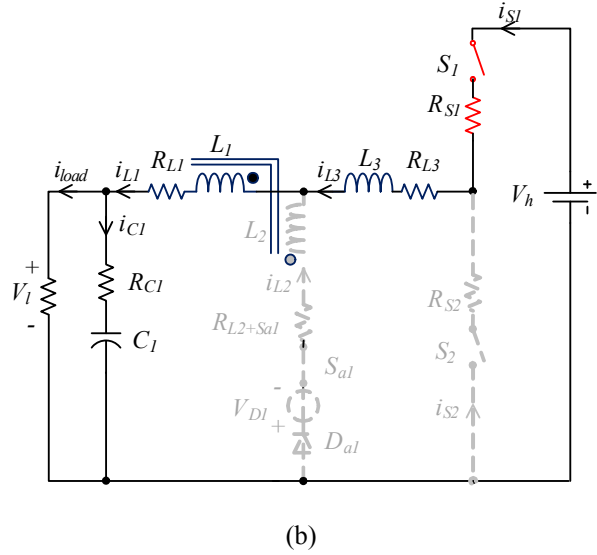
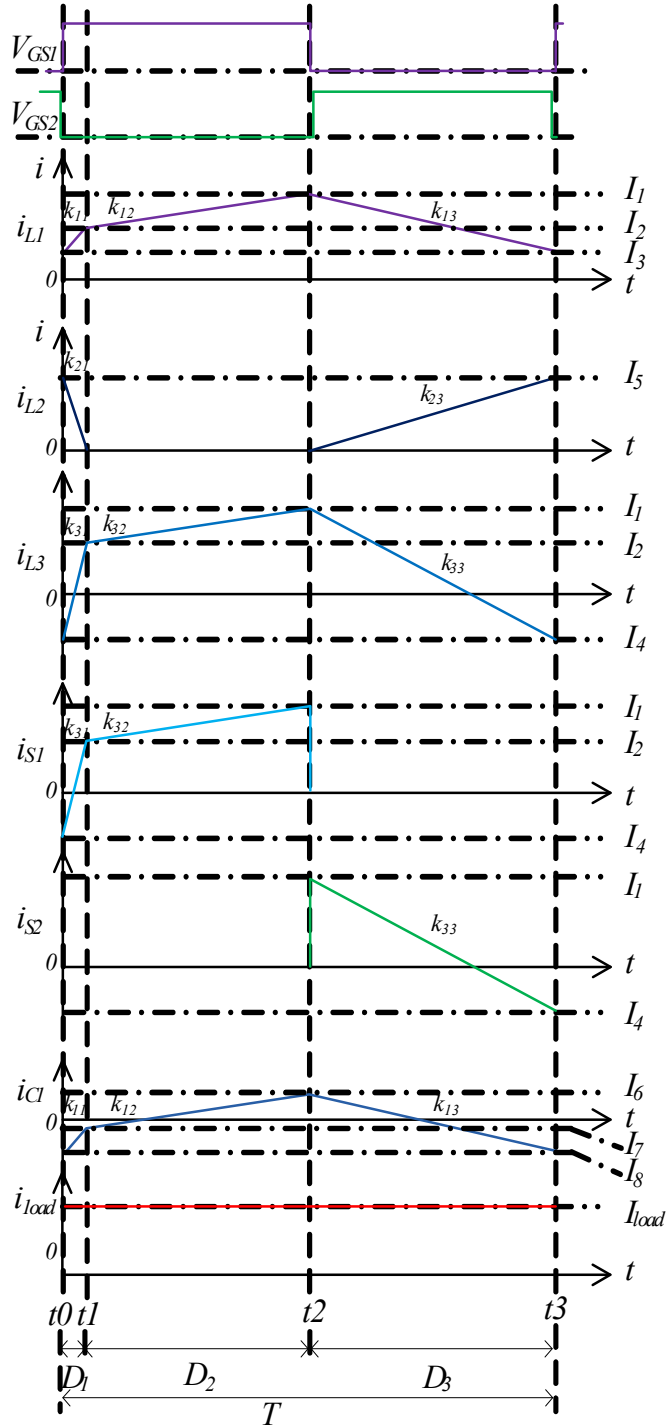


Figure 3 Equivalent circuits for each operation mode of buck mode. (a) Mode 1, t_0-t_1 ; (b) Mode 2, t_1-t_2 ; (c) Mode 3, t_2-t_3 (continued) (see online version for colours)



The theoretical waveforms of i_{L1} , i_{L2} , i_{L3} , i_{S1} , i_{S2} , i_{C1} and i_{load} are shown in Figure 4, where D_1 , D_2 and D_3 are the duty ratios for mode 1, mode 2, and mode 3, respectively; T is the switching period; k_j indicates a different current slope at a different mode; and i denotes the inductor number and j denotes the mode number. Based on these waveforms, the conduction losses for each branch can be calculated, and the total conduction losses and efficiency are also obtained. The detailed calculating procedures are as follows.

Figure 4 Waveforms of i_1 , i_2 and i_3 at steady state of buck mode (see online version for colours)



1 *Inductor current slopes*

From the work of Zhang and Sen (2003), the inductor current slopes can be obtained as follows.

$$k_{11} = \frac{V_h(L_2 + \sqrt{L_1 L_2}) - V_l(L_3 + L_2)}{(L_1 + L_2 + 2\sqrt{L_1 L_2})L_3} \quad (1)$$

$$k_{12} = \frac{V_h - V_l}{L_1 + L_3} \quad (2)$$

$$k_{13} = -\frac{V_l(L_3 + L_2)}{(L_1 + L_2 + 2\sqrt{L_1 L_2})L_3} \quad (3)$$

$$k_{21} = \frac{-V_h(L_1 + \sqrt{L_1 L_2}) + V_l(\sqrt{L_1 L_2} - L_3)}{(L_1 + L_2 + 2\sqrt{L_1 L_2})L_3} \quad (4)$$

$$k_{22} = 0 \quad (5)$$

$$k_{23} = \frac{V_l(\sqrt{L_1 L_2} - L_3)}{(L_1 + L_2 + 2\sqrt{L_1 L_2})L_3} \quad (6)$$

$$k_{31} = \frac{V_h}{L_3} - \frac{V_l(L_2 + \sqrt{L_1 L_2})}{(L_1 + L_2 + 2\sqrt{L_1 L_2})L_3} \quad (7)$$

$$k_{32} = \frac{V_h - V_l}{L_1 + L_3} \quad (8)$$

$$k_{33} = -\frac{V_l(\sqrt{L_1 L_2} + L_2)}{(L_1 + L_2 + 2\sqrt{L_1 L_2})L_3} \quad (9)$$

where all the inductor currents are only related to the input and output voltages and the inductances. Hence, the load and switching frequency variations will not result in the changes of all the current slopes.

2 *D_1, D_2 and D_3*

Based on the waveforms of i_{L1} and i_{L3} , it can be seen that the variations of i_{L1} and i_{L3} in a switching period are zero, so the equations can be obtained as:

$$\begin{cases} (k_{11}D_1 + k_{12}D_2 + k_{13}D_3)*T = 0 \\ (k_{21}D_1 + k_{22}D_2 + k_{23}D_3)*T = 0 \\ D_1 + D_2 + D_3 = 1 \end{cases} \quad (10)$$

Then,

$$D_1 = \frac{k_{33}(k_{12} - k_{13}) - k_{13}(k_{32} - k_{33})}{(k_{11} - k_{13})(k_{32} - k_{33}) - (k_{31} - k_{33})(k_{12} - k_{13})} \quad (11)$$

$$D_2 = \frac{k_{33}(k_{11} - k_{13}) - k_{13}(k_{31} - k_{33})}{(k_{12} - k_{13})(k_{31} - k_{33}) - (k_{32} - k_{33})(k_{11} - k_{13})} \quad (12)$$

$$D_3 = 1 - D_1 - D_2 \quad (13)$$

It can be seen that the duty ratios of each mode only depend on the inductor current slopes, so they are also independent with the load current and switching frequency, i.e. the duty ratios will not change in this converter with fixed inductances, and fixed input and output voltages.

3 Current values I_i of each component

I_i denotes the current values of different components at different time points, and the detailed references are shown in Figure 4. All current values can be expressed as the function of I_1 , current slopes k_{ij} , duty ratios D_i . Since the average of i_{L1} is equal to the output current I_{load} , we can obtain an equation of I_1 and I_{load} as:

$$\frac{I_3 + I_2}{2} D_1 + \frac{I_2 + I_1}{2} D_2 + \frac{I_1 + I_3}{2} D_3 = I_{load} \quad (14)$$

Then,

$$\begin{aligned} & \frac{2I_1 - (2k_{12}D_2 + k_{11}D_1)T}{2} D_1 \\ & + \frac{2I_1 - k_{12}D_2T}{2} D_2 \\ & + \frac{2I_1 - (k_{12}D_2 + k_{11}D_1)T}{2} (1 - D_1 - D_2) = I_{load} \end{aligned} \quad (15)$$

So, we can get

$$\begin{aligned} I_1 &= f_1(I_{load}, T) \\ &= I_{load} + \frac{(k_{11}D_1 + k_{12}D_2) - (k_{11} - k_{12})D_1D_2}{2} T \end{aligned} \quad (16)$$

where I_1 is positive correlation to the load current, and direct correlation to the switching frequency. It is because the two variables are independent of each other, and k_{11} , k_{12} , D_1 , and D_2 are independent of I_{load} and T .

From the waveforms shown in Figure 4 and equation (16), the other current values are expressed as follows.

$$\begin{aligned} I_2 &= I_1 - k_{12}D_2T \\ &= I_{load} + \frac{(k_{11}D_1 - k_{12}D_2) - (k_{11} - k_{12})D_1D_2}{2} T \end{aligned} \quad (17)$$

$$\begin{aligned}
I_3 &= I_1 - (k_{12}D_2 + k_{11}D_1)T \\
&= I_{load} - \frac{(k_{11}D_1 + k_{12}D_2) + (k_{11} - k_{12})D_1D_2}{2}T
\end{aligned} \tag{18}$$

$$\begin{aligned}
I_4 &= I_1 - (k_{32}D_2 + k_{31}D_1)T \\
&= I_{load} + \frac{(k_{11}D_1 - k_{12}D_2) - (k_{11} - k_{12})D_1D_2 - 2k_{31}D_1}{2}T
\end{aligned} \tag{19}$$

$$I_5 = -k_{21}D_1T \tag{20}$$

$$I_6 = I_1 - I_{load} = \frac{(k_{11}D_1 + k_{12}D_2) - (k_{11} - k_{12})D_1D_2}{2}T \tag{21}$$

$$I_7 = I_2 - I_{load} = \frac{(k_{11}D_1 - k_{12}D_2) - (k_{11} - k_{12})D_1D_2}{2}T \tag{22}$$

$$I_8 = I_3 - I_{load} = -\frac{(k_{11}D_1 + k_{12}D_2) + (k_{11} - k_{12})D_1D_2}{2}T \tag{23}$$

Thus, it can be also obtained that I_1 , I_2 , I_3 and I_4 , is a first-order linear function of two independent variables such as I_{load} and T . Furthermore, from equations (16)–(18), it can be seen that i_{L1} consists of a DC part and an AC part, where the DC part is I_{load} , and the AC part is only related to T . Also, the AC part at any load condition is the same while the switching frequency is fixed. Since i_{L3} is the sum of i_{S1} (t_0 – t_2) and i_{S2} (t_2 – t_3), the AC parts of i_{S1} and i_{S2} also remain the same at any load with a fixed switching frequency. Based on equations (20)–(23), we can conclude that the waveforms of i_{L2} and i_{C1} with a fixed switching frequency always remain the same, no matter what the load is, including no load.

4 Power losses of each branch, and total power losses

From the current waveforms, as shown in Figure 4, we can get the power losses for each branch, such as S_1 , S_2 , L_1 , L_2 and C_1 . To simplify the calculations, the parasitic resistance of L_3 is contained in S_1 and S_2 branches, as shown in Figure 2.

The power losses of L_1 branch are equal to $I_{L1_rms}^2 R_{L1}$, where the rms current I_{L1_rms} can be expressed as below.

$$\begin{aligned}
I_{L1_rms}^2 &= \frac{1}{T} \int_{t_0}^{t_3} i_{L1}^2(t) dt \\
&= \frac{1}{T} \left(\int_{t_0}^{t_1} i_{L1}^2(t) dt + \int_{t_1}^{t_2} i_{L1}^2(t) dt + \int_{t_2}^{t_3} i_{L1}^2(t) dt \right)
\end{aligned} \tag{24}$$

where

$$\begin{aligned}
\int_{t_0}^{t_1} i_{L1}^2(t) dt &= \int_0^{D_1T} i_{L1}^2(t) dt = \int_0^{D_1T} \left(\frac{I_2 - I_3}{D_1T} t + I_3 \right)^2 dt \\
&= \frac{1}{3} \left(\frac{I_2 - I_3}{D_1T} \right)^2 (D_1T)^3 + \frac{I_2 - I_3}{D_1T} I_3 (D_1T)^2 + I_3^2 D_1T \\
&= \frac{I_3^2 + I_3 I_2 + I_2^2}{3} D_1T
\end{aligned} \tag{25}$$

Using the similar method, it can be obtained as below.

$$I_{L1_rms}^2 = \frac{I_3^2 + I_3 I_2 + I_2^2}{3} D_1 + \frac{I_2^2 + I_2 I_1 + I_1^2}{3} D_2 + \frac{I_1^2 + I_1 I_3 + I_3^2}{3} D_3 \quad (26)$$

Then

$$P_{LOSS_L1} = I_{L1_rms}^2 R_{L1} \quad (27)$$

The power losses of S_1 branch are

$$P_{LOSS_S1} = \left(\frac{I_4^2 + I_4 I_2 + I_2^2}{3} D_1 + \frac{I_2^2 + I_2 I_1 + I_1^2}{3} D_2 \right) \times (R_{S1} + R_{L3}) \quad (28)$$

The power losses of S_2 branch are

$$P_{LOSS_S2} = \frac{I_1^2 + I_1 I_4 + I_4^2}{3} D_3 (R_{S2} + R_{L3}) \quad (29)$$

The power losses of L_2 branch consist of two parts. One is the conduction losses of S_{a1} and L_2 , and another part is caused by the forward voltage drop of D_{a1} . The total losses are

$$P_{LOSS_L2} = \frac{I_5^2 (D_1 + D_3)}{3} R_{L2+S_{a1}} + \frac{I_5 (D_1 + D_3)}{3} V_{Da1} \quad (30)$$

The power losses of C_1 branch are expressed as:

$$P_{LOSS_C1} = \left(\frac{I_8^2 + I_8 I_7 + I_7^2}{3} D_1 + \frac{I_7^2 + I_7 I_6 + I_6^2}{3} D_2 + \frac{I_6^2 + I_6 I_8 + I_8^2}{3} D_3 \right) \times R_{C1} \quad (31)$$

From the above analyses, it can be seen that the power losses of each branch are a binary quadratic function of load current I_{load} and switching period T (i.e. the reciprocal of the switching frequency f_{sw}). Thus, the total power losses are also a binary quadratic function of I_{load} and f_{sw} :

$$P_{LOSS_ALL} = f_2 (I_{load}, f_{sw}) = P_{LOSS_L1} + P_{LOSS_L2} + P_{LOSS_S1} + P_{LOSS_S2} + P_{LOSS_C1} \quad (32)$$

5 Efficiency

Based on the analyses above, the efficiency can be obtained:

$$Efficiency = \frac{P_{output}}{P_{output} + P_{LOSS_ALL}} = \frac{V_1 I_{load}}{V_1 I_{load} + f_2 (I_{load}, f_{sw})} \quad (33)$$

Substituting equations (27)–(32) into equation (33), the detailed efficiency equation as the function of I_{load} and f_{sw} can be easily derived, but it is not given here because the equation is very long and complicated.

The above efficiency equation is based on the assumed condition that ZVS conditions are always obtained at any f_{sw} and I_{load} . However, ZVS conditions are likely to be difficult to be achieved with high I_{load} and f_{sw} in the practical converter. Hence, the efficiency equation is not suitable for the converter without ZVS. The relationship of f_{sw} , I_{load} , and the constraints for ZVS should be discussed, which is given in the next section.

2.3 The relationship of f_{sw} , I_{load} , with constraints for ZVS

The ZVS conditions are achieved by charging and discharging the snubber capacitors with the energy stored in L_3 at t_0 , and it must be enough to achieve ZVS conditions. From equation (19), it can be seen that I_4 (negative in buck mode) rises as I_{load} rises, i.e. the energy stored in L_3 will descend. Also, the heaviest load will result in the least stored energy, so the maximum load is the worst situation for ZVS. The following inequality can be used to express the constraints for ZVS.

$$I_4 \leq -\sqrt{\frac{(C_{a1} + C_{a2})V_h^2}{L_3}} \quad (34)$$

Substituting equation (19) into equation (34), the constraints for ZVS can be expressed as the relationship of f_{sw} and I_{load}

$$f_{sw} \leq \frac{(k_{11}D_1 - k_{12}D_2) - (k_{11} - k_{12})D_1D_2 - 2k_{31}D_1}{2\left(-\sqrt{\frac{(C_{a1} + C_{a2})V_h^2}{L_3}} - I_{load}\right)} \quad (35)$$

It is also known that ZVS is very critical to obtain high efficiency. Thus, ZVS needs to be guaranteed even if the converter works under a variable frequency, i.e. inequality (35) is a mandatory condition for the variable frequency control in this topology.

3 Simulation results and discussions

Simulation was first performed to validate the feasibility of the system before experiments were conducted. To be consistent with the laboratory hardware set-up on a scaled-down system, a 1 kW system was chosen. The practical parameters, such as the parasitic resistances, the inductances, the input/output voltages, and so on, are presented in Table 1. The used MOSFETs, like S_1 , S_2 , and S_{a1} , are CoolMOS IPW60R041C6, made by Infineon. Diode D_{a1} is 60EPU02PbF made by Vishay. The magnetic core of L_1 and L_2 is 00K5530E060 and 00K3007E060 is used for L_3 , all produced by Magnetics.

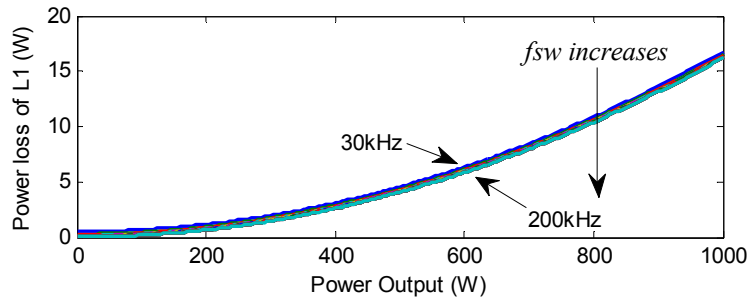
Substituting the parameters into equations (27)–(31), the simulated power loss for each branch is shown in Figure 5. The switching frequency f_{sw} is from 30 kHz to 200 kHz, and the step size is 10 kHz. The direction of frequency increasing is indicated by a black solid arrow in each figure. In Figure 5a and 5b, we can see that the power losses of branches S_1 and L_1 are not optimised obviously as f_{sw} increases, and they are mainly determined by the load current, i.e. the output power. In Figure 5c, when the output power is low, the power losses of branch S_2 are reduced as f_{sw} increases, especially in the low frequency region (30–70 kHz). In Figure 5d, it can be easily seen that the power loss of branch L_2 remains a constant with a fixed f_{sw} , even if the output power is zero. Moreover, the power losses of branch L_2 , dominated in the light load total power losses, are bad for efficiency improvement at a light load condition. The power losses of this branch, however, are also reduced as f_{sw} increases. In Figure 5e, the power losses of C_1 are also decreased while f_{sw} increases. The feature is similar to that of branch L_2 , but the maximum power losses are very small (less than 0.4 W under a 1 kW output power).

Thus, loss of C_1 can be neglected when analysing efficiencies. In addition, summing the power losses of all branches, the total power losses are obtained as shown in Figure 5f, where the total power losses can be reduced as f_{sw} increases, i.e. the efficiency will be improved if f_{sw} increases. The simulated efficiency curves are shown in Figure 6.

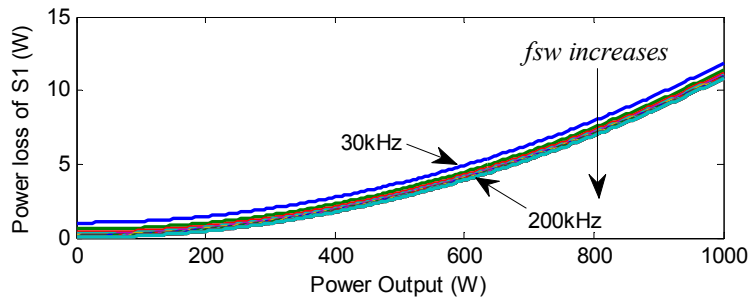
Table 1 The practical parameters of the converter

Symbol	Values
V_h	100 V
V_1	50 V
L_1	80.7 μ H
L_2	0.78 μ H
L_3	1.3 μ H
R_{L1}	40.5 m Ω
R_{L2}	8 m Ω
R_{L3}	4 m Ω
R_{S1}	50 m Ω
R_{S2}	50 m Ω
R_{Sa1}	50 m Ω
R_{C1}	30 m Ω
V_{Da1}	0.8 V

Figure 5 Power loss of each branch and all power loss with several frequencies. (a) Power loss of L_1 . (b) Power loss of S_1 . (c) Power loss of S_2 . (d) Power loss of L_2 . (e) Power loss of C_1 . (f) All power loss (see online version for colours)

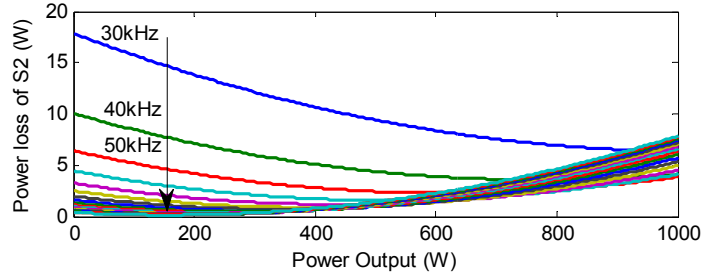


(a)

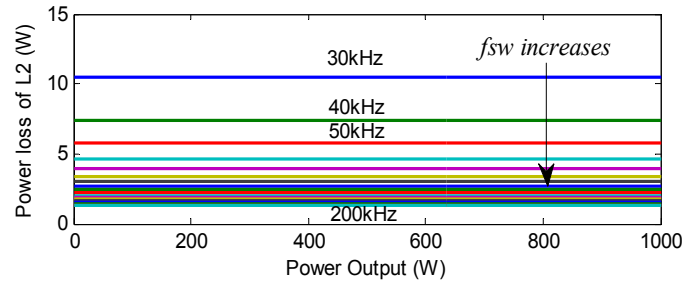


(b)

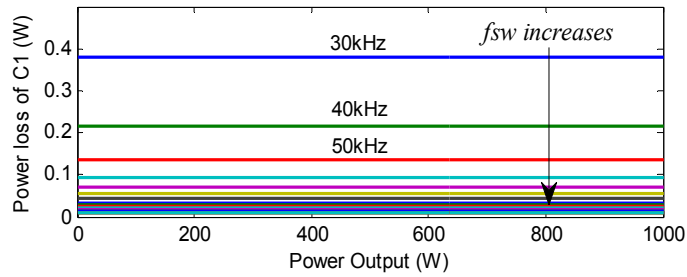
Figure 5 Power loss of each branch and all power loss with several frequencies. (a) Power loss of L_1 . (b) Power loss of S_1 . (c) Power loss of S_2 . (d) Power loss of L_2 . (e) Power loss of C_1 . (f) All power loss (continued) (see online version for colours)



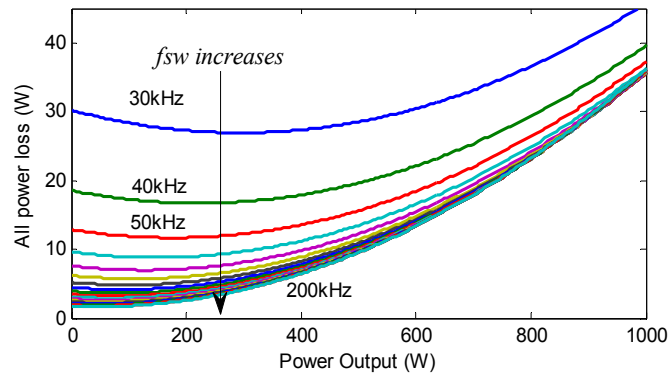
(c)



(d)

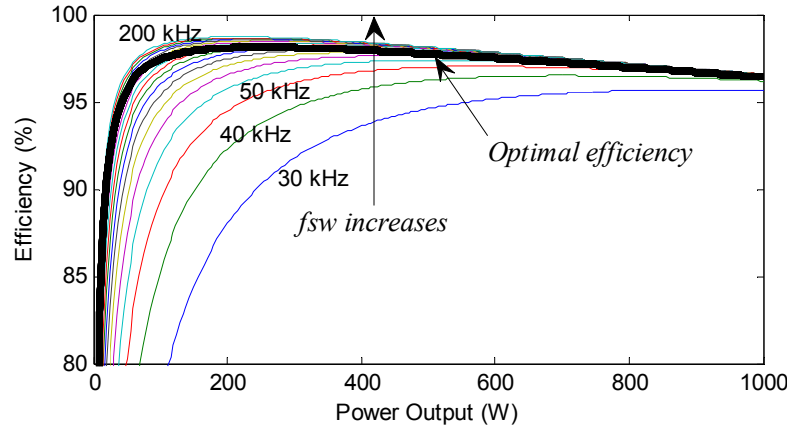


(e)



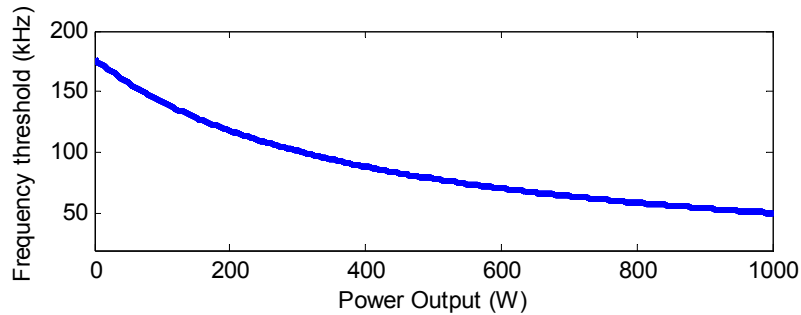
(f)

Figure 6 Efficiency curves at a variable f_{sw} and the optimal efficiency (see online version for colours)



However, all the above simulated results are based on the assumption that ZVS are always achieved. In fact, from equation (35), there is a different frequency threshold for different output power (Figure 7). When f_{sw} is greater than the frequency threshold, ZVS will not be obtained, so the efficiency equations are not suitable. In order to achieve both ZVS conditions and optimal efficiencies, especially at a light load condition, it can be concluded that the converter should operate along the switching frequency threshold, i.e. the converter always operates under the critical ZVS mode. The optimal efficiency curve is also shown with a thick-black line in Figure 6.

Figure 7 Frequency threshold for achieving ZVS conditions (see online version for colours)



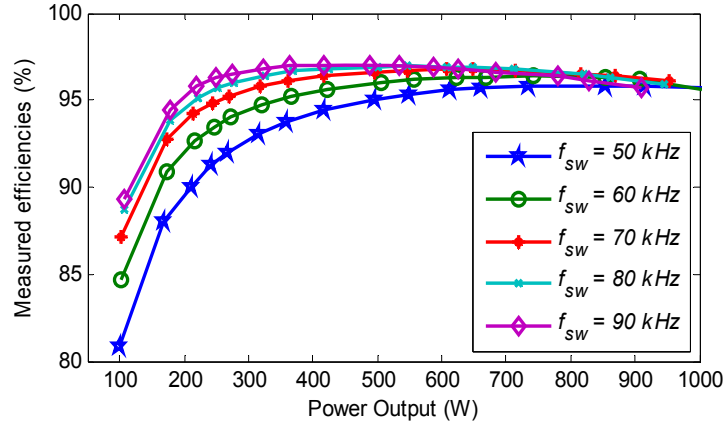
4 Experimental results of efficiency

To verify the above analyses, the scaled-down prototype converter will operate with several fixed f_{sw} (50 kHz, 60 kHz, 70 kHz, 80 kHz and 90 kHz), and the efficiency curves are measured, as shown in Figure 8. It can be seen that

- 1 The efficiencies within most of the total output power are increased with an increasing f_{sw} .

- 2 The optimising effect is particularly obvious at a light load and not obvious at a heavy load. When operating at a heavy load, the efficiency will decrease with the increasing f_{sw} because of the failure of soft-switching.
- 3 The improved effect will become smaller when the frequency becomes higher. When f_{sw} increases from 50 kHz to 60 kHz, the optimising effect on the efficiency is especially obvious. However, the optimising effect becomes very small when f_{sw} increases from 80 kHz to 90 kHz, which is also the reason that we do not present the efficiencies with a much higher f_{sw} .

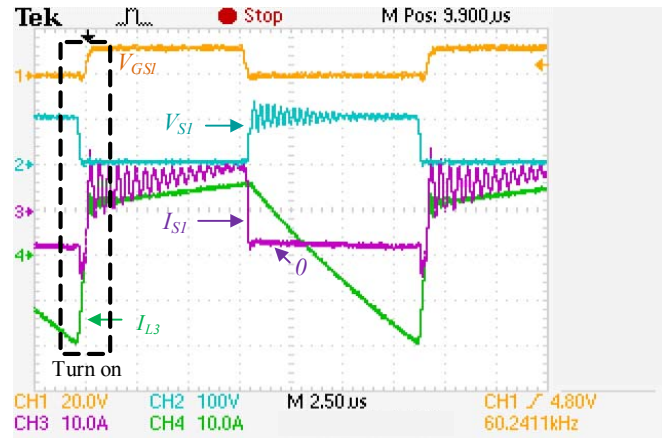
Figure 8 Experimental efficiencies at several fixed frequencies (see online version for colours)



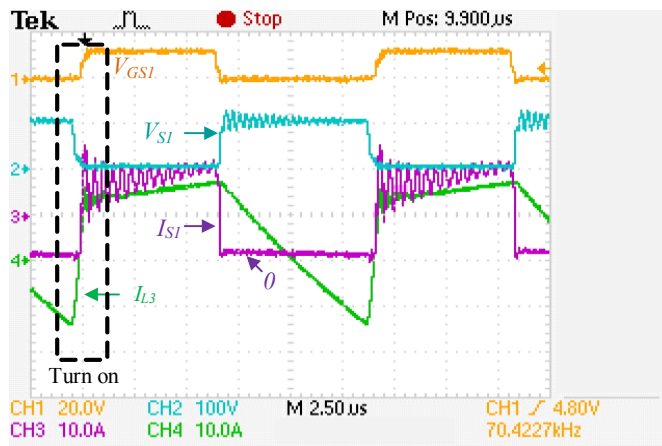
From the simulated efficiency waveforms of Figure 6, we can see that the efficiencies are increased with an increasing f_{sw} . The improved effect of efficiencies becomes smaller when the load becomes heavier. The improved effect becomes smaller when the switching frequency becomes higher. Hence, based on the analyses, it can be concluded that the experimental efficiency waveforms (Figure 8) have validated the feasibility of the simulated efficiency waveforms (Figure 6). Moreover, the other theoretical analyses about the efficiency in Sections 2 and 3 are verified.

In addition, the efficiency with a higher frequency will be decreased when the load is high, and it is because ZVS conditions are not achieved. Initially, the proposed converter is designed with f_{sw} at 50 kHz, and ZVS conditions are always achieved at this f_{sw} . However, ZVS conditions, especially the turn-on processes, are likely difficult to achieve when f_{sw} is increasing. For example, when the output power is 710 W, the experimental waveforms of S_1 and i_{L3} at 60 kHz, 70 kHz and 80 kHz, as shown in Figure 9, demonstrates the completion effect of ZVS conditions. In Figure 9a, f_{sw} is 60 kHz, and ZVS conditions have already been achieved since i_{S1} goes negative before S_1 is triggered on. In Figure 9b, f_{sw} is 70 kHz, and ZVS conditions are critical to be achieved because i_{S1} is zero when V_{S1} decreases to zero and S_1 is triggered on. In Figure 9c, f_{sw} is 80 kHz, and ZVS conditions are not obtained because V_{S1} does not decrease to zero when S_1 is triggered on. Although i_{L3} goes negative before S_1 is triggered on, the stored energy in L_3 is also not enough. So V_{S1} is just reduced slightly from V_h , not to zero. From Figure 9, it can also be seen that the energy stored in L_3 before S_1 is triggered on will reduce when f_{sw} increases from 60 kHz to 80 kHz. Hence, we can conclude that ZVS conditions are difficult to be achieved as f_{sw} increases.

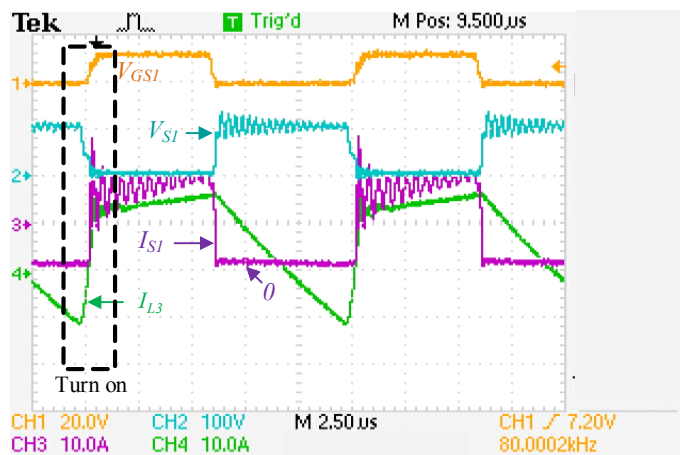
Figure 9 The experimental waveforms of S_1 and i_{L3} at different f_{sw} . (a) $f_{sw} = 60$ kHz. (b) $f_{sw} = 70$ kHz. (c) $f_{sw} = 80$ kHz (see online version for colours)



(a)



(b)



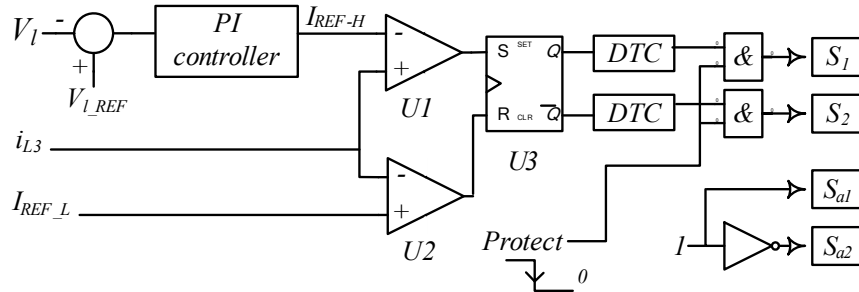
(c)

5 The proposed control method

From the above discussion, in order to obtain both high efficiency and ZVS conditions, the converter needs to be controlled by a Variable Frequency Controller (VCF). In general, VCF can be easily implemented by a lookup table. However, when the load condition varies, there is a delay before adjusting the frequency, and then a novel peak-valley current control method is proposed and some simulated results are given to illustrate the validities.

Taking the buck mode as an example, the valley value of i_{L3} is employed to determine whether the ZVS conditions are implemented, and the peak value of i_{L3} is used to control the output objective (output voltage or current). The simplified diagram of the proposed control method is shown in Figure 10, where $U1$ and $U2$ are two comparators; $U1$ is used to control the peak value and $U2$ is used to control the valley value. $U3$ (a RS flip-flop) is employed to generate the driving pulse. DTC means the dead time control, i.e. on-delays before turn-on of S_1 and S_2 . The two AND gates are used to lock the driving pulse because of some protections. V_{l-REF} is the reference of the output voltage. I_{REF-H} is the upper threshold. If i_{L3} is bigger than I_{REF-H} , S_1 will be turned off and S_2 will be turn on. Similarly, I_{REF-L} is the lower threshold, which determines the completion of ZVS. If i_{L3} is smaller than I_{REF-L} , S_1 will be turned on and S_2 will be turn off. If I_{REF-L} is equal to the critical value for ZVS, the ZVS conditions will be always implemented at any load condition by using the proposed control methods. Hence, the converter will automatically operate along the switching frequency threshold given in Figure 7.

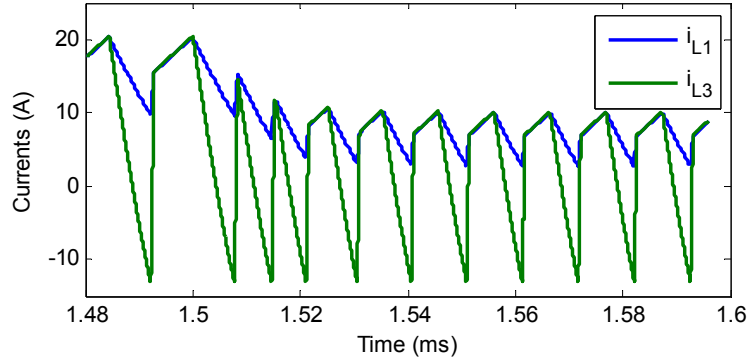
Figure 10 The simplified control diagram in buck mode



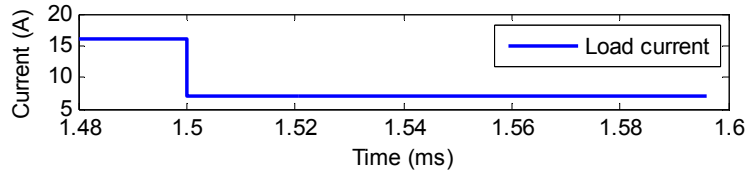
Using the parameters (Table 1) the simulated model of the proposed converter with the proposed control method is built with SIMULINK software, where the converter operates in buck mode with constant output voltage. The simulated results of step load resistances between $8\ \Omega$ and $4\ \Omega$ are presented in Figures 11 and 12.

Figure 11 shows dynamic responses of a step-down load. In Figure 11a, it can be seen that the valley value of i_{L3} remains a constant even if the load resistance increases. We can see that f_{sw} also increases with the step-down load except the dynamic adjusting process. Figure 11b shows the output current. In addition, Figure 12 shows responses of a step-up load. Figure 12a shows that the valley value of i_{L3} does not change even if the load resistance decreases. It also illustrates that f_{sw} decreases with the step-up load. Hence, we can conclude that the feasibility of the proposed control method is validated.

Figure 11 Dynamic response of a step-down load in buck mode (see online version for colours)

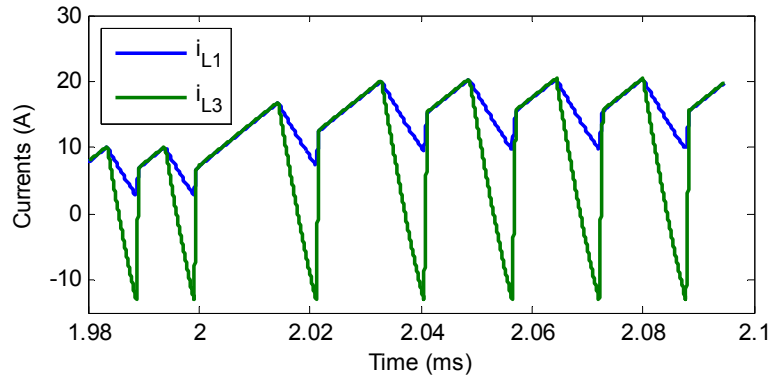


(a)

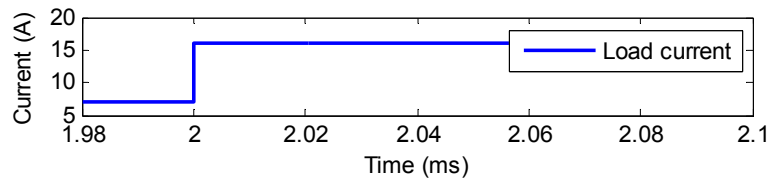


(b)

Figure 12 Dynamic response of a step-up load in buck mode (see online version for colours)



(a)



(b)

In addition, the proposed control method is not only suitable for buck mode, but also for boost mode. Swapping of the threshold inputs of $U1$ and $U2$ is needed, and the peak value is employed to determine whether the ZVS conditions are achieved, and the valley value is for controlling the output objective (output voltage or current). Moreover, it is very meaningful that the proposed method can also be used for other ZVS topologies like interleaved structures (Yu and Lai, 2008), the ZVS principles of which are similar to those of the proposed topology, and the efficiencies of these interleaved structures can be improved by employing the proposed approach.

6 Conclusion

In this paper, we proposed a control method to implement a variable frequency control of a non-isolated bidirectional soft-switching DC-DC converter for HESS. The detailed theoretical analyses about the power losses of each branch were presented and from the simulated results, the power losses can be reduced by increasing the switching frequency when load power reduces. Based on the 1 kW prototype, the efficiency at several fixed switching frequencies was measured, which verifies the efficiency improvement with the higher switching frequency. However, too high switching frequency will result in the failure of ZVS conditions. The threshold frequencies (also the optimised frequencies) for critically achieving ZVS conditions are also presented. Finally, in order to achieve both ZVS condition and high efficiency at all load conditions, a control method was proposed to implement variable frequency control along the threshold frequency. This control is very simple to be implemented. The simulated results validated the feasibility of this method. The authors believe that this control method is suitable for other ZVS converters to improve efficiency over a large load range.

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