Single-Stage Resonant Battery Charger With Inherent Power Factor Correction for Electric Vehicles

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***Abstract*—This paper presents the study of a single-stage onboard battery charger for electric vehicle (EV) and plug-in hybrid EV (PHEV) applications. The topology had never been seen in any literature or patents but is employed in the NLG5 charger made by Brusa Elektronik AG. We thoroughly analyzed the topology and thought it would be beneficial to publish it so that advanced work can be done based on the existing structure. The charger directly transfers power from the alternating current (ac) to the battery side; thus, the bulky electrolytic capacitor in a traditional two-stage charger is eliminated. Power factor correction (PFC) is inherently achieved; thus, the control becomes very simple. In addition, all the power switches work at a zero-current switching (ZCS) condition to reduce the switching loss. The charger charges the battery with a sinusoidal-like charging current instead of a constant direct current. However, this current waveform has minimal impact on the battery life and efficiency, as demonstrated by other studies. Hence, having the advantages of high efficiency, compact size, easy control, and no need of an electrolytic capacitor, the topology is suitable for the PHEV and the pure EV onboard charging applications.**

***Index Terms*—Battery charger, electrolytic capacitor, film capacitor, plug-in electric vehicle (EV), single stage, zero-current switching (ZCS).**

I. Introduction

RECENTLY, plug-in hybrid electric vehicles (PHEV) and pure electric vehicles (EV) are being commercialized to reduce fossil-fuel consumption and reduce greenhouse gas emissions. In both PHEV and EV, a single-phase 3 kW $\sim$ 6 kW onboard charger is usually installed; thus, the high-power traction battery pack can be charged through a utility power outlet [1], [2]. The well-known topology of an onboard charger is the two-stage structure. A front stage, which is usually a boost converter, is adopted to perform power factor correction (PFC) for less line loss and alternating-current (ac) power capacity [3]. A second stage, which is usually a high-efficiency isolated direct-current (dc)–dc converter, is adopted to meet the safety regulations and to control the charging current [4]. In a traditional two-stage battery charger, the charging current is usually a constant dc; thus, the output power is constant. While the input ac supply outputs a sinusoidal power, a dc-link capacitor, with the value of which from a few hundred microfarads to a few thousand microfarads, is needed as an energy buffer tank [5], [6]. Usually, the dc-link capacitor is an electrolytic capacitor with a short lifetime, which is not preferable for an onboard charger. A film capacitor is a good substitute. However, for the value required in a traditional two-stage charger, a film capacitor is too expensive and bulky. It is important to reduce the capacitor value; thus, a film capacitor can be used for long lifetime usage without increasing the cost and the size.

Reducing the dc-link capacitor has already become a new research area in the recent years. There are several ways to eliminate the big capacitor in a charger. One method is adding an active ripple energy filter [7], [8]. For this kind of method, usually, an additional buck boost converter is adopted as the filter, by charging and discharging a second capacitor to filter out the input power ripple. In this way, the battery-charging current keeps constant, and the value of the dc-link capacitor can be reduced to about 1/10, as compared with that without using the active filter [7]. The drawback is that the system becomes more complex. The extra converter brings additional cost and loss. In addition, 1/10 of the original capacitor value is still in the hundred-microfarad level, which is still expensive for a film capacitor.

Based on the previous research work, twice the power-frequency current ripple does not have an obvious adverse effect on the efficiency and the life performance of the lithium-ion batteries [9]–[11]. An alternative method is to charge the battery by a sinusoidal-like dc current [12]–[19]. With this method, the input ac power directly goes to the battery side without an energy buffer. In theory, the dc-link capacitor can be completely removed from the circuit.

Still, the charger can be a two-stage topology with some changes in configuration and control strategy [12], [13]. However, using a single-stage topology to realize the PFC, isolation and battery-charging current control sounds more attractive for its simplicity and lower cost [14]–[19]. Most of the single-stage topologies are only for low-power applications under 1 kW. They are hard to be scaled up to high-power applications for PHEV and EV onboard chargers. For high-power applications, we only found one publication in which a single-stage multiresonant inductive charger is proposed [19]. The efficiency is 91% at full load, which is acceptable but quickly drops (70% at 20% load) when the output power reduces. Aside from that, the parameter and controller designs of a multiresonant converter are complicated.

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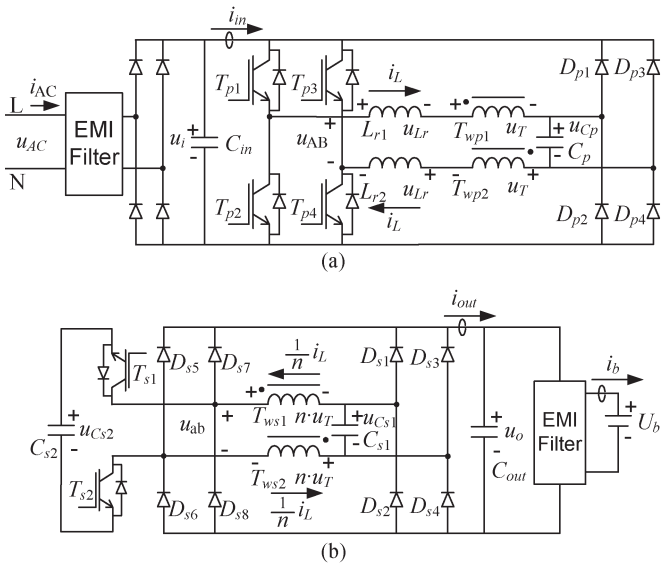

Fig. 1. Topology of single-stage EV battery charger. (a) Primary- and (b) secondary-side structures.

In this paper, a single-stage resonant battery-charger topology is introduced and analyzed. The topology is shown in Fig. 1. The leakage inductance of the isolation transformer forms a resonant circuit with voltage-clamped capacitors. All the power switches are turned on and off at a zero-current condition; thus, both the switching loss and the electromagnetic interference (EMI) are reduced. The secondary switches only work for a short time when the ac line voltage is lower than the battery voltage (after it converts to the primary side); thus, the loss caused by the secondary switches is very small. The transfer of energy from the ac source to the battery comes from two parts. One part of the energy is stored in the transformer leakage inductance first and then transferred to the battery. The other part of the energy is directly transferred from the ac source to the battery. By combining both of the energy transfer patterns, the presented topology possesses a high-power output capability. This topology has been used in a battery charger that is made by Brusa. The design guidelines are given to calculate all the parameters of the resonant circuit. Also, we verified the efficiency of the charger by experiment. It is about 92%–93% from 20%–100% output power.

II. Battery-Charger Topology and Operating Principles

The topology that is shown in Fig. 1 is not easy to understand at first sight. However, after we analyzed it, we found that it is pretty simple. $T_{\rm wp1}$, $T_{\rm wp2}$, $T_{\rm ws1}$, and $T_{\rm ws2}$ are the four windings of an isolation transformer. This is the only one magnetic component in the circuit, aside from the input and output EMI filters. The primary-to-secondary-turn ratio is $1:n$. L_{r1} and L_{r2} are the leakage inductance values that are shown at the primary side. C_p, C_{s1}, and C_{s2} are three voltage-clamped capacitors. $T_{p1} \sim T_{p4}$, T_{s1}, and T_{s2} are insulated-gate bipolar transistor (IGBT) switches. The switching sequence is shown in Fig. 2. u_i is the rectified ac input voltage. Approximately, it is the absolute value of $u_{\rm ac}$. U_b is the battery voltage. For switching frequency around 100 kHz, u_i can be regarded as a

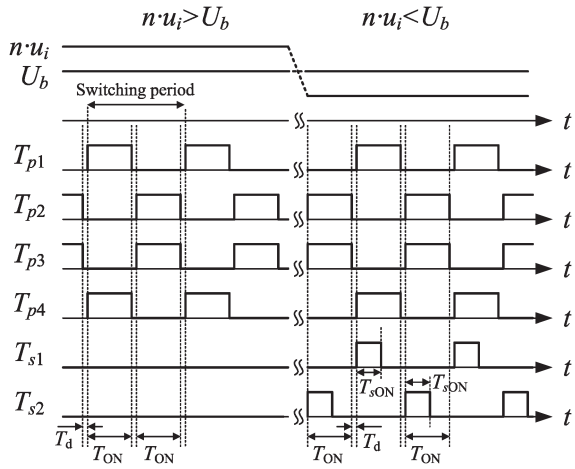

Fig. 2. Switching sequence.

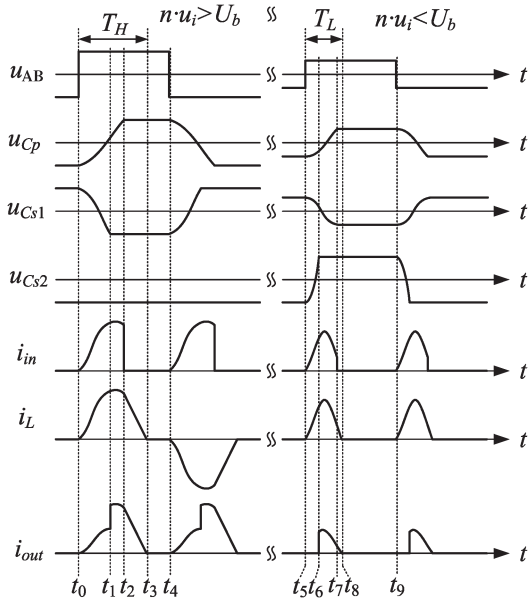

Fig. 3. Key voltage and current waveforms.

constant value in one switching period. When $n \cdot u_i > U_b$, T_{s1} and T_{s2} do not work. L_{r1} and L_{r2} resonate with C_p and C_{s1}. The resonant makes the u_{Cp} switch between $-u_i$ and u_i. When $n \cdot u_i \le U_b$, at the beginning of each primary-side switching period, T_{s1} and T_{s2} are turned on for a short time $T_{\rm sON}$ to put C_{s2} into the resonant circuit. This action is like a boost method to make u_{Cp} swing between $-u_i$ and u_i at a low input voltage. The key point of this topology is that the input current $i_{\rm in}$ charges C_p with a voltage change $2u_i$ in each $T_{\rm ON}$ period. For each switching period, there are two $T_{\rm ON}$ periods. Thus, the integral of $i_{\rm in}$ in one switching period is $4C_p \cdot u_i$. After $C_{\rm in}$ and the EMI filter, the average input current is

$$i_{\rm AC} = 4f \cdot C_p \cdot u_{\rm AC} \tag{1}$$

where f is the switching frequency.

The input current $i_{\rm AC}$ is proportional to the input voltage when f is fixed. At a certain charging current, the PFC is achieved just by keeping the switching frequency constant. The battery-charging current can be controlled by changing the switching frequency; the higher the frequency, the larger the charging current.

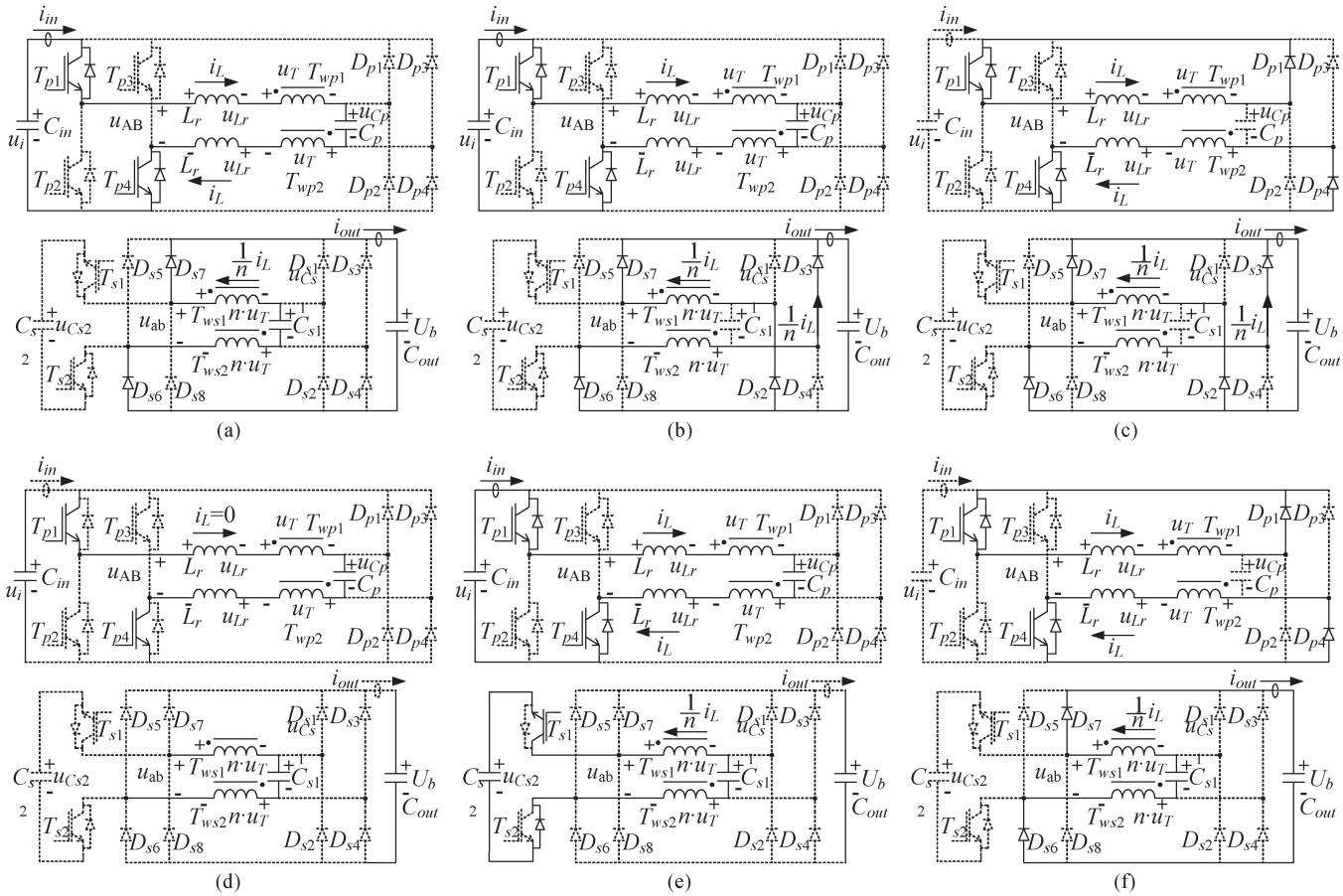

Fig. 4. Equivalent circuit for stages (a) H1 and L2, (b) H2, (c) H3, (d) H4 and L4, (e) L1, and (f) L3.

The key voltage and current waveforms under both $n \cdot u_i > U_b$ and $n \cdot u_i < U_b$ conditions are shown in Fig. 3. The analysis will be discussed in two parts, one for $n \cdot u_i > U_b$ and the other for $n \cdot u_i < U_b$. To simplify the problem, the following approximations and design rules are made:

1) In the transformer design, the magnetizing inductance is about a hundred times of the leakage inductance. The magnetizing current is negligible compared with the resonant current. The transformer model that is expressed by the four windings $T_{\rm wp1}$, $T_{\rm wp2}$, $T_{\rm ws1}$, and $T_{\rm ws2}$ in Fig. 1 will be regarded as the ideal ones.
2) The parasitic resistance in the circuit is neglected.
3) The transformer and circuit parameters are symmetrical. A common symbol will be used if they have the same value. For example, we used u_{Lr} to represent the voltage on L_{r1} and L_{r2}.
4) Voltage u_i on input capacitor $C_{\rm in}$ is constant in one switching period. Voltage u_o on output capacitor $C_{\rm out}$ is constant and is equal to the battery voltage U_b.
5) The values of the two capacitors C_p and C_{s1} are designed by (2). C_{s2} is designed to be much smaller than C_{s1}. The reason will be discussed later. Under this design, we have $\Delta u_{Cp} = -n \cdot \Delta u_{Cs1}$ when the current flows on both C_p and C_{s1}, i.e.,

$$C_p = n^2 \cdot C_{s1}. \tag{2}$$

A. Input AC Voltage is High ($n \cdot u_i > U_b$)

In this condition, L_{r1}, L_{r2}, C_p, and C_{s1} form a resonant circuit. At time t_0, the initial conditions are $u_{\rm AB}(t_{0-}) = -u_i$, $u_{\rm AB}(t_{0+}) = u_i$, $u_{Cp}(t_0) = -u_i$, $u_{Cs1}(t_0) = U_b$, and $i_L(t_0) = 0$. Because of the symmetry, we only give the analysis for $t_0 \sim t_4$, which is a half switching period.

Stage H1 ($t_0 \sim t_1$): At time t_0, T_{p2} and T_{p3} are turned off, and T_{p1} and T_{p4} are turned on [see Fig. 4(a)]. $u_{\rm AB}$ switches from $-u_i$ to u_i. In this stage, diodes D_{s6} and D_{s7} are on; thus, $u_{\rm ab} = U_b$. The circuit equations are succeedingly listed. The first equation is acquired through the voltage equations on both the side of the transformer and its voltage ratio n. C_p and C_{s1} are discharged first and then charged again by the resonant. Because $n \cdot u_i > U_b$ and the relation between C_p and C_{s1}, which is given in (2), u_{Cs1} will be clamped to $-U_b$ at time t_1 before u_{Cp} is clamped to u_i, i.e.,

$$\begin{cases} n \cdot u_i - U_b = 2n \cdot u_{Lr} + n \cdot u_{Cp} - u_{Cs1} \\ u_{Lr} = L_r \cdot \frac{di_L}{dt} \\ u_{Cp} = u_{C_p}(t_0) + \frac{1}{C_p} \int\limits_{t_0}^{t} i_L \cdot dt \\ u_{Cs1} = u_{C_{s1}}(t_0) - \frac{1}{C_{s1}} \int\limits_{t_0}^{t} \frac{1}{n} i_L \cdot dt \\ i_{\rm in} = i_L \\ i_{\rm out} = i_L / n. \end{cases} \tag{3}$$

Stage H2 ($t_1 \sim t_2$): At time t_1, u_{Cs1} is clamped to $-U_b$, and diodes D_{s2} and D_{s3} turn on [see Fig. 4(b)]. The connection of the secondary windings $T_{\rm ws1}$ and $T_{\rm ws2}$ changes from a series to a parallel. The output current doubles to $2i_L/n$. u_{Cp} is continuously charged until t_2. In this stage, the circuit equations are

$$\begin{cases} n \cdot u_i - 2U_b = 2n \cdot u_{Lr} + n \cdot u_{Cp} \\ u_{Lr} = L_r \cdot \frac{di_L}{dt} \\ u_{Cp} = u_{C_p}(t_1) + \frac{1}{C_p} \int_{t_1}^{t} i_L \cdot dt \\ u_{Cs1} = -U_b \\ i_{\rm in} = i_L \\ i_{\rm out} = 2i_L/n. \end{cases} \tag{4}$$

Stage H3 ($t_2 \sim t_3$): At time t_2, u_{Cp} is clamped to u_i, diodes D_{p1} and D_{p4} turn on, and $i_{\rm in}$ drops to zero [see Fig. 4(c)]. Both C_p and C_{s1} are clamped; thus, there is no current through them. The reflected battery voltage is applied on the leakage inductance. Current i_L linearly reduces. The circuit equations for this stage are

$$\begin{cases} u_{Lr} = L_r \cdot \frac{di_L}{dt} = -\frac{1}{n} U_b \\ u_{Cp} = u_i \\ u_{Cs1} = -U_b \\ i_{\rm in} = 0 \\ i_{\rm out} = 2i_L/n. \end{cases} \tag{5}$$

Stage H4 ($t_3 \sim t_4$): At time t_3, i_L reduces to zero [see Fig. 4(d)]. All the diodes naturally turn off. After t_3, the resonant stops. u_{Cp} and u_{Cs1} stay for u_i and $-U_b$, respectively, and i_L keeps at zero. At time t_4, T_{p1} and T_{p4} will be turned off, and T_{p2} and T_{p3} will be turned on at zero current. Zero-current switching (ZCS) is achieved. The initial conditions for the next half switching period are $u_{\rm AB}(t_{4-}) = u_i$, $u_{\rm AB}(t_{4+}) = -u_i$, $u_{Cp}(t_4) = u_i$, $u_{Cs1}(t_4) = -U_b$, and $i_L(t_4) = 0$. They are symmetrical with the initial conditions at time t_0. Similar procedures of stages $H1 \sim H4$ will be repeated. u_{Cp} swings between $-u_i$ and u_i; thus the integral of the input current $i_{\rm in}$ is equal to $2C_p \cdot u_i$ in each $T_{\rm ON}$ period.

B. Input AC Voltage is Low ($n \cdot u_i < U_b$)

When the input voltage is low, let us look back at (3) to think what will happen. In (3), when $n \cdot u_i > U_b$, the left side of the first equation, which can be seen as a forced component, is above zero. According to the resonant circuit current direction, it means that the forced component is giving energy into the resonant circuit. However, when $n \cdot u_i < U_b$, the forced component is below zero. It means that the forced component is taking energy away from the resonant circuit. In this situation, the swing amplitude of u_{Cp} will gradually attenuate. The input current will reduce, and the PFC cannot be realized. To keep u_{Cp} swing between $-u_i$ and u_i at low input ac voltage, a switching action in the secondary side is performed as a boost function. To analyze the procedure, we begin at time t_5 with the following initial conditions: $u_{\rm AB}(t_{5-}) = -u_i$, $u_{\rm AB}(t_{5+}) = u_i$, $u_{Cp}(t_5) = -u_i$, $u_{Cs1}(t_5) = u_x$, $u_{Cs2}(t_5) = -U_b$, and $i_L(t_5) = 0$. The value of u_x will be discussed later.

Stage L1 ($t_5 \sim t_6$): At time t_5, T_{p2} and T_{p3} are turned off, and T_{p1} and T_{p4} are turned on [see Fig. 4(e)]. At the same time, T_{s1} is turned on at a zero-current condition. u_{Cs2} is charged through T_{s1} and the antiparallel diode of T_{s2}. The initial voltage of u_{Cs2} is $-U_b$. The equations for this stage are shown as

$$\begin{cases} n \cdot u_i - u_{Cs2} = 2n \cdot u_{Lr} + n \cdot u_{Cp} - u_{Cs1} \\ u_{Cs2} = u_{Cs2}(t_5) + \frac{1}{C_{s2}} \int_{t5}^{t} \frac{1}{n} i_L \cdot dt \\ u_{Lr} = L_r \cdot \frac{di_L}{dt} \\ u_{Cp} = u_{C_p}(t_5) + \frac{1}{C_p} \int_{t_5}^{t} i_L \cdot dt \\ u_{Cs1} = u_{C_{s1}}(t_5) - \frac{1}{C_{s1}} \int_{t_5}^{t} \frac{1}{n} i_L \cdot dt. \end{cases} \tag{6}$$

Comparing with stage H1, at time t_5, the left side of the first equation changes from $n \cdot u_i - U_b$ to $n \cdot u_i + U_b$. The leakage inductance is charged at a much higher voltage. Because C_{s2} is smaller than C_{s1}, at time t_6, u_{Cs2} will be clamped at U_b before u_{Cs1} and u_{Cp} are clamped. In this stage, both u_{Cs1} and u_{Cs2} are smaller than U_b; thus, there is no output current. Energy is taken from input capacitor $C_{\rm in}$ and stored into L_r. The extra energy from $C_{\rm in}$ will make C_p swing to u_i in the next stage.

Stage L2 ($t_6 \sim t_7$): At time t_6, u_{Cs2} is charged and clamped to U_b [see Fig. 4(a)]. D_{s6} and D_{s7} are on. Current through T_{s1} reduces to zero. T_{s1} can be turned off at a zero-current condition at any time after t_6 and before t_9. For simplicity, $T_{s\rm ON}$ can be designed to a fixed value, which is greater than $t_6 - t_5$. Equations in this stage are similar to that in stage H1, only the initial state is different. By replacing t_0 in (3), using t_6, we can have the equations for stage L2.

Stage L3 ($t_7 \sim t_8$): At time t_7, u_{Cp} is charged and clamped to u_i. D_{p1} and D_{p4} turn on [see Fig. 4(f)]. Different from stage H3, only u_{Cp} is clamped at time t_7. After t_7, there is no input current from $C_{\rm in}$. The transformer output current flows into both $C_{\rm out}$ and C_{s1}. The equations for this stage are

$$\begin{cases} -U_b = 2n \cdot u_{Lr} - u_{Cs1} \\ u_{Lr} = L_r \cdot \frac{di_L}{dt} \\ u_{Cs1} = u_{C_{s1}}(t_7) - \frac{1}{C_{s1}} \int_{t_7}^{t} \frac{1}{n} i_L \cdot dt \\ i_{\rm out} = i_L/n. \end{cases} \tag{7}$$

Stage L4 ($t_8 \sim t_9$): At time t_9, i_L reduces to zero [see Fig. 4(d)]. All the diodes turn off naturally. After t_9, the resonant stops. u_{Cp} and u_{Cs1} stay for u_i and $-u_x$, respectively, and i_L keeps at zero. At time t_9, T_{p1} and T_{p4} will be turned off, and T_{p2}, T_{p3}, and T_{s2} will be turned on at zero current. ZCS is achieved. The initial conditions for the next half switching period are $u_{\rm AB}(t_{9-}) = u_i$, $u_{\rm AB}(t_{9+}) = -u_i$, $u_{Cp}(t_9) = u_i$, $u_{Cs1}(t_9) = -u_x$, and $i_L(t_9) = 0$. They are symmetrical with the initial conditions at time t_5. Similar procedures of stages L1 $\sim$ L4 will be repeated.

The initial voltage u_x is slightly larger than u_i/n. In stages L1 and L2, we have $\Delta u_{Cp} = -n \cdot \Delta u_{Cs1}$. In stage L3, $\Delta u_{Cp} = 0$, and $\Delta u_{Cs1} < 0$. Therefore, in stages L1 $\sim$ L3,

$\Delta u_{Cp} = 2u_i < -n \cdot \Delta u_{Cs1} = 2n \cdot u_x$. This makes a small difference when the input voltage is only slightly smaller than U_b/n. In this case, u_x will be clamped to U_b. However, u_x does not matter very much. As long as u_{Cp} can swing between $-u_i$ and u_i, the PFC can be realized. In the aforementioned analysis, we assumed at the end of stage L1, u_{Cs2} is equal to U_b. However, if u_i is too low, u_{Cs2} cannot swing to U_b. Thus, there is no energy output to the battery side. The energy provided by $C_{\rm in}$ in stage L1 ensures the swing of u_{Cp} between $-u_i$ and u_i. In this case, the input current still satisfies (1).

III. Design Guidelines

Since the analyzed topology is not similar to any other ones that are publicly available, it is not easy to understand how to design the parameters. Here, the design guidelines are given. Based on these guidelines, all the important parameters of the charger can be easily calculated.

A. Primary-Side Capacitance C_p

According to the previous analysis, the input current is $4f \cdot C_p \cdot u_{\rm AC}$. Thus, the input power is

$$P_{\rm in} = 4f \cdot C_p \cdot U_{\rm AC}^2 \tag{8}$$

where $U_{\rm AC}$ is the root-mean-square (RMS) value of the input ac voltage. According to (8), higher input voltage corresponds to higher input power. Thus, we need specify a minimum input voltage for the charger to get a full output power. Below the specified input voltage, the charger works at a derating condition. Then, if the desired maximum output power is $P_{\rm max}$, we can design C_p by

$$C_p = \frac{P_{\rm max}}{4f_{\rm max} \cdot \eta \cdot U_{\rm AC\,min}^2} \tag{9}$$

where $U_{\rm AC\,min}$ is the RMS value of the minimum input ac voltage for full output power, $f_{\rm max}$ is the system maximum switching frequency, and η is the estimated efficiency of the charger. We can use 90% as the charger's efficiency to get a conservative value.

By improving the switching frequency, we can use a smaller capacitor. However, we need to consider the switching loss. Because the converter works at zero current but not at zero-voltage switching condition, the output capacitor is charged and discharged at each switching action, which brings some loss. We need to set a maximum switching frequency according to the device characteristics.

B. Secondary-Side Capacitance C_{s1} and C_{s2}

Once C_p is designed, we can calculate C_{s1} using (2). The reason is explained here. We can see from (3) that, when $n \cdot u_i > U_b$ and their values are close, in stages H1 and H2, the resonant circuit can get very little energy from the forced component $n \cdot u_i - U_b$. With a smaller C_{s1} value, u_{Cs1} changes faster and is clamped earlier. When u_{Cs1} is clamped to $\pm U_b$, the forced component changes to $n \cdot u_i - 2U_b$, as shown in (4). Energy flows out of the resonant circuit and goes into $C_{\rm out}$. If u_{Cs1} is clamped to $\pm U_b$ earlier, the energy in the resonant circuit may reduce after a cycle. In this case, the swing amplitude of u_{Cp} will reduce, and the input-current shape gets distorted. Thus, C_{s1} should be large enough. However, for each switching action, C_{s1} discharges and charges. A larger C_{s1} means larger circulating energy, which brings more loss. Thus, C_{s1} should be designed to the smallest value that can ensure the swing of u_{Cp} between $-u_i$ and u_i for the whole range when $n \cdot u_i \geq U_b$. We have then solved stages H1 $\sim$ H3 and acquired $C_{s1} \geq C_p/n^2$.

The design of C_{s2} is similar. On one side, C_{s2} should be big enough. Thus, there is enough energy stored in L_r in stage L1 to make u_{Cp} swing between $-u_i$ and u_i. On the other side, a larger C_{s2} means larger circulating energy loss. To ensure that u_{Cp} can be clamped to u_i, we solved it in the following way: if there is no clamp circuit, when i_{Lr} reduces to zero in stage L2, u_{Cp} should be greater than u_i. We can calculate the relationship between C_{s2} and C_{s1} according to the aforementioned equations and analysis. The solution is that the following inequalities should be satisfied for all input-voltage values when $n \cdot u_i < U_b$:

$$\begin{cases} \text{when } \frac{2}{3}k_1 \leq k_2 < 1 : k_1 \geq 0.25 - \left(k_2 - \frac{1}{2}\right)^2 \\ \text{when } 0 \leq k_2 < \frac{2}{3}k_1 : k_1 \geq 0 \end{cases} \tag{10}$$

where $k_1 = C_{s2}/C_{s1}$, and $k_2 = n \cdot u_i/U_b$.

When $2 \cdot k_1/3 \leq k_2 < 1$, stages L1 $\sim$ L4 occur. When $k_2 < 2 \cdot k_1/3$, the input voltage is very low that u_{Cs2} cannot swing from $-U_b$ to U_b. The amplitude of u_{Cs2} will reduce under this condition, as mentioned in Section II. From (10) and the aforementioned analysis, we can get the optimal C_{s2} value as

$$C_{s2} = 0.25C_{s1}. \tag{11}$$

C. Leakage Inductance L_r

The design of leakage inductance L_r should consider two aspects. One is that L_r should be small enough that stages H1 $\sim$ H4 and stages L1 $\sim$ L4 can be finished in the half switching period at $f_{\rm max}$. The other is that a smaller L_r will cause a larger resonant current. The current stress increases when L_r reduces. We define $T_H = t_3 - t_0$ and $T_L = t_8 - t_5$. The minimum $T_{\rm ON}$ value should always be larger than T_H and T_L. By solving the aforementioned equations, we found that T_L is always smaller than T_H. Only T_H is concerned in the design of leakage inductance L_r. The solution for T_H is

$$T_H = \left\{ \sqrt{2}\cos^{-1}\left[\frac{2 - k_2 + (k_2 - 1)\sqrt{2(k_2 - 1)}}{k_2^2 - 2k_2 + 2}\right] + \cos^{-1}\left(1 - \frac{2}{k_2}\right) + \sqrt{2}(k_2 - 1)\right\}\sqrt{C_p L_r}. \tag{12}$$

For stage H1 $\sim$ H4, k_2 is always greater than 1. According to (10), lower battery voltage means larger k_2, which increases T_H. If we want to maintain the same output power, which

means the same switching period, we should reduce L_r to make sure $T_H < T_{\rm ON}$. This will increase the current stress. In the design, a minimum battery voltage $\min\{U_b\}_{\rm fullpower}$ for full power output should be set. If the battery voltage is lower than $\min\{U_b\}_{\rm fullpower}$, the switching frequency should be reduced to ensure the ZCS condition. In this case, the charger works at a derated condition. As a battery charger, the maximum k_2 value is usually less than 5, which means that $\min\{U_b\}_{\rm fullpower}$ is about 1/4 about the maximum output voltage for this topology. When $1 < k_2 < 5$, (12) is very similar to a linear function. To simplify the design procedure, we use curve fitting to get an approximate result, i.e.,

$$T_H = (1.28k_2 + 1.58)\sqrt{C_p L_r} \le \frac{1}{2f_{\max}}. \tag{13}$$

Thus, we can design L_r by the following:

$$L_r \le \frac{1}{4f_{\max}^2 \cdot (1.28k_{2\max} + 1.58)^2 \cdot C_p} \tag{14}$$

where $k_{2\max} = n \cdot \max\{u_i\}/\min\{U_b\}_{\rm fullpower}$.

D. Transformer Ratio n

The design of transformer ratio n is related to the charger's input- and output-voltage specifications. For higher efficiency, we prefer that the charger works at the $n \cdot u_i > U_b$ stage. However, if we use higher ratio n to expand the $n \cdot u_i > U_b$ range, $k_{2\max}$ will increase. Thus, we need to reduce L_r to achieve the same switching frequency for the desired power. The current stress will increase, which could decrease the efficiency. Usually, we can design n to make U_b at the middle section of $n \cdot u_i$ for better efficiency.

The aforementioned design guidelines can give the optimal parameters in theory. In the real system, we need to choose more conservative values to ensure the current shape for less total harmonic distortions (THDs). C_{s1} and C_{s2} should be slightly larger and L_r be slightly smaller. The operation of the secondary switches should start when $n \cdot u_i$ is still slightly larger than U_b.

IV. Simulation and Experimental Results

A. Charger Specifications and Parameters

To show more comprehensive waveforms, and verify the aforementioned analysis, we did simulation and experiment based on a Brusa NLG513 charger. The main specifications [20] are listed in Table I. Although the input-voltage range is $90 \sim 264$ V, the minimum input voltage for full output power is 208 VAC. The input capacitor $C_{\rm in}$ is only 3 μF; thus, a film capacitor can be easily adopted. Table II gives a comparison of the key parameters that are calculated by design guidelines and the corresponding values in the Brusa charger. We believe these parameters have been carefully optimized by Brusa. The parameters for the resonant circuit agree well with the values that are calculated by the aforementioned design guidelines.

TABLE I
Charger Specifications and Circuit Parameters

Spec / Parameter	Value
Input voltage range	90~264 V
Maximum input power	3.68 kW
Maximum output power	3.3 kW
Output voltage[*1]	260~520V
Power density	~ 9W/ in^3
n	2.15
$f$max	~ 150 kHz
C_{in}	3 µF
C_{out}	6 µF

[*1]Full power output voltage. Below this voltage, reduced power.

TABLE II
Resonant Circuit Parameters

Parameter	Design value	Brusa value
C_p	0.141 µF	0.136 µF
C_{s1}	0.0305 µF	0.0285 µF
C_{s2}	0.0076 µF	0.0075 µF
L_r	3.5 µH	2.9 µH

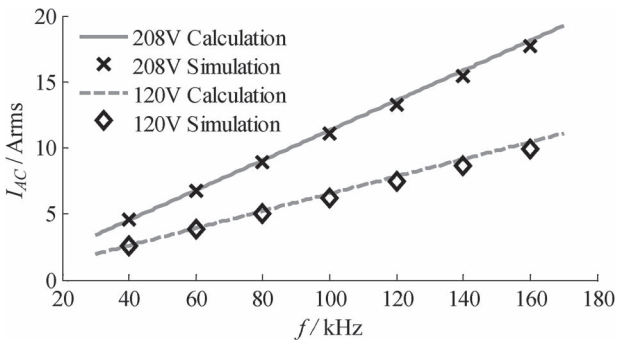

Fig. 5. Input current vs. switching frequency.

B. Simulation Results

Simulation was carried out using MATLAB Simulink to verify the analysis. First, the relation between the input current and the switching frequency is simulated under both 208- and 120-VAC input voltage. The comparison with the analytical results is shown in Fig. 5. The simulation values are slightly smaller than the calculated results. This is because there is some voltage drop on the EMI filter and the rectifier diode bridge in the simulation.

The partial enlarged waveforms for $n \cdot u_i > U_b$ and $n \cdot u_i < U_b$ are shown in Fig. 6. They agree well with the aforementioned analysis results that are shown in Fig. 3. Thus, according to the aforementioned analysis, all the IGBT and the diodes are operated at a ZCS status. We did not give the overall outline of the waveforms here. They are almost the same with the experimental results, which will be shown in the succeeding section.

At a 208-VAC input voltage and a 3.3-kW output power, the RMS value of i_L and the THD of the input current $i_{\rm AC}$ under different C_{s1} and C_{s2} values are simulated and shown in Fig. 7. When C_{s1} and C_{s2} are smaller than the designed

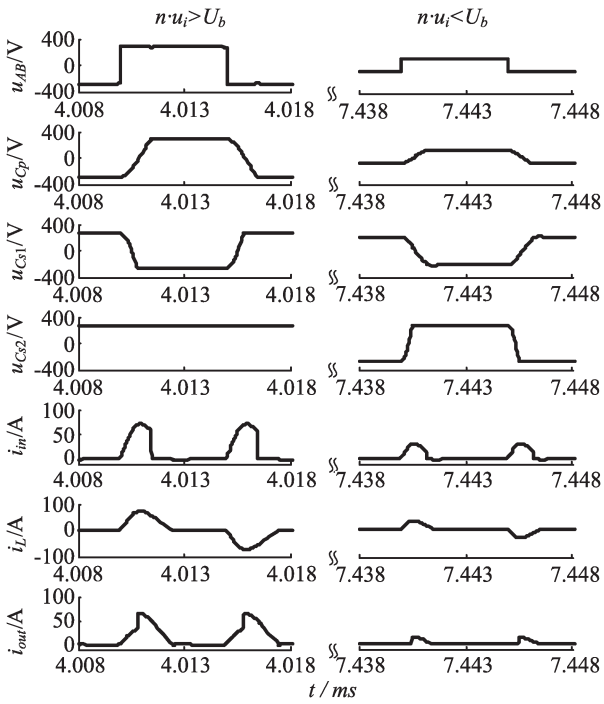

Fig. 6. Simulation of the key voltage and current waveforms.

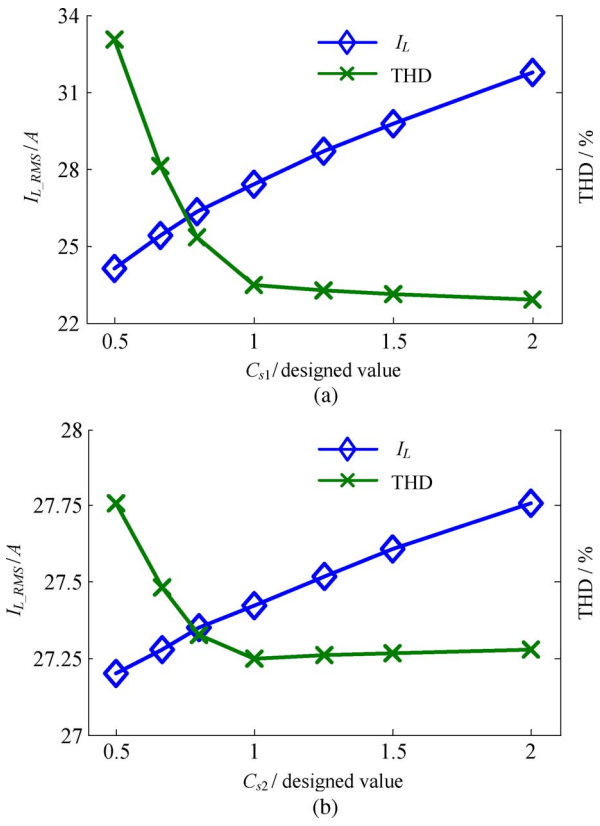

Fig. 7. RMS of i_L and THD of $i_{\rm AC}$. (a) Different C_{s1} and (b) C_{s2} values.

value from (2) and (11), respectively, the THD of the input current $i_{\rm AC}$ obviously increases. When C_{s1} and C_{s2} increase, the RMS value of i_L continuously increases. It means that there is a larger amount of circulating energy in the circuit, which brings more losses. At the designed C_{s1} and C_{s2} values, the input-current THD is almost minimized at the smallest i_L RMS value. Thus, higher efficiency and better input-current quality can be obtained at the same time.

C. Experimental Results

First, the typical waveforms were measured under a 208-VAC input and a 300-V/10-A output, and they are shown in Fig. 8. Fig. 8(a) shows the driving signals of T_{p1} and T_{s1}. T_{p1} continuously switches at a fixed frequency. T_{s1} only switches for a short time when $u_{\rm in}$ is low. The outline of i_L is also shown in Fig. 8(a). When T_{s2} switches, the amplitude of i_L slightly increases. In the simulation, we found that, if we choose a larger C_{s2}, the increase will be bigger; thus, the loss increases. If we choose a smaller C_{s2} value, the increase will be too small; thus, u_{Cp} cannot swing from $-u_i$ to u_i. Fig. 8(b) shows the voltage of the three resonant capacitors. u_{Cp} swings from $-u_i$ to u_i all the time; thus, the input current is proportional to the input voltage. The PFC is realized. Fig. 8(c) gives the waveform of input voltage $u_{\rm AC}$, input current $i_{\rm AC}$, and output charging current i_b. $i_{\rm AC}$ is in phase with $u_{\rm AC}$. Unlike traditional two-stage chargers, the output current i_b is a sinusoidal-like dc current, which contains an output-current ripple at twice the power grid frequency.

The efficiency, the THD, and the power factor under the 240-VAC input with different output voltage and power values were measured using the YOKOGAWA WT1600 power analyzer. The results are shown in Fig. 9. We can see that the efficiency is about 92% $\sim$ 93% from 20% $\sim$ 100% output power. High efficiency was achieved not only in the high-power output region but also in the low-power output region. This is due to the relative low switching frequency at the low output power. The input ac quality is also good. At the 3.3-kW output power, the THD is less than 3%, and the power factor is about 0.997.

D. Comparison With Some Other Topologies

A comparison between the analyzed single-stage resonant topology (A) and the other two topologies are given in Table III. One is a popular state-of-art two-stage topology (B), which incorporates an interleaved PFC front-stage [6] and an LLC resonant dc/dc converter [4]. The other is a recently developed electrolytic-capacitor-free topology (C) [12]. Compared with topology B, both A and C avoid the using of electrolytic capacitors. In addition, the control is simpler. For both A and C, the switching frequency and the duty ratio are kept constant at a certain charging condition. The switching frequency or the duty ratio (for A and C, respectively) changes only when the battery voltage and the required output power changes. Meanwhile, because there is no electrolytic capacitor as the energy buffer, as well as the resonant procedure for soft switching, the current stresses on power semiconductor switches for A and C are higher than B. This lowers the efficiency and limits the very high-power ($>$ 10 kW) applications. In topology A, although more diodes are used, high efficiency is achieved by the IGBT, which is usually more cost effective than using a metal–oxide–semiconductor field-effect transistor (MOSFET).

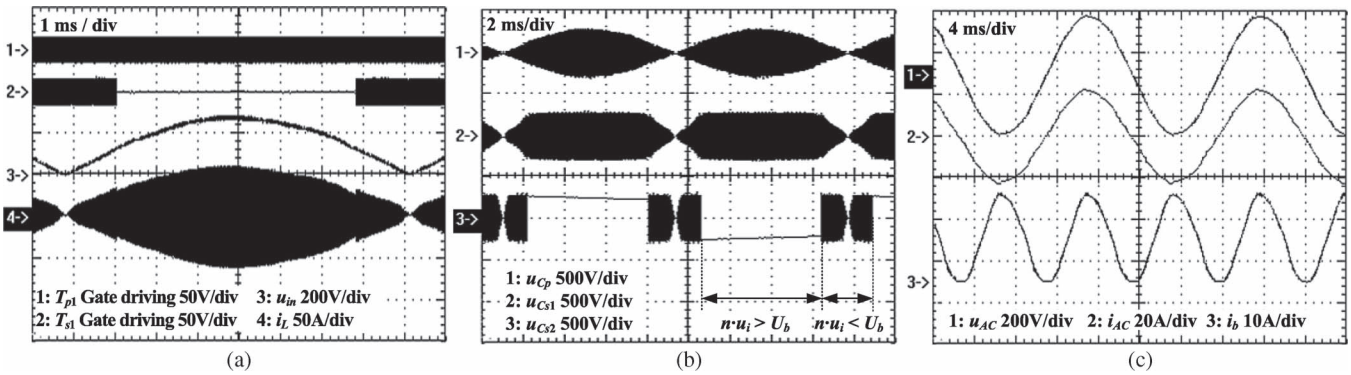

Fig. 8. Simulation of the key voltage and current waveforms. (a) Driving signals and transformer winding current. (b) Resonant-capacitor voltages. (c) Input- and output-current values.

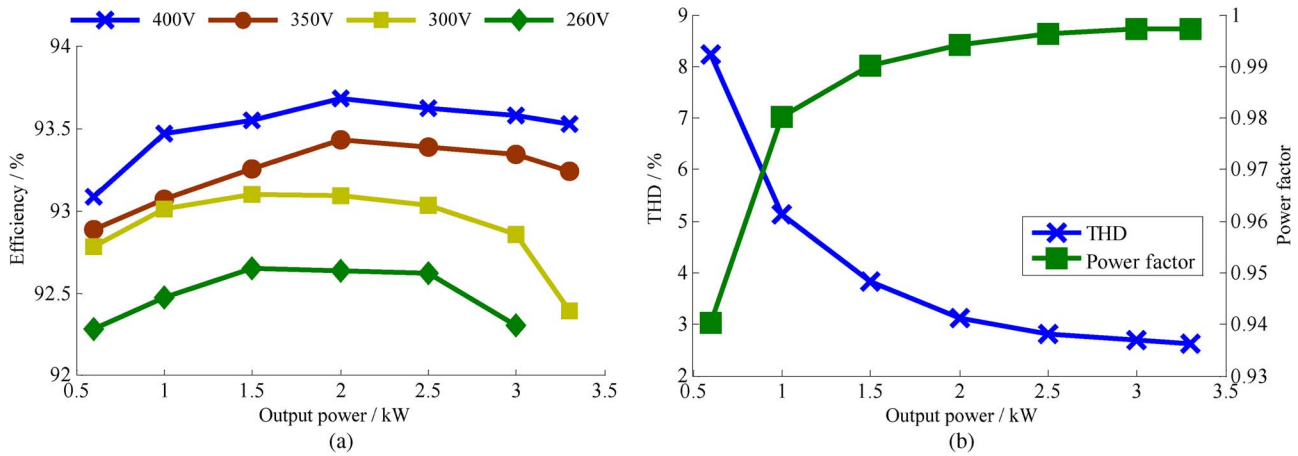

Fig. 9. Input current quality. (a) Efficiency under different output voltage. (b) Input current THD and power factor.

TABLE III
COMPARISON OF DIFFERENT TOPOLOGIES

	A: Single-stage resonant	B: Interleaved PFC and LLC	C: LLC and Buck-boost
Main switches	6 IGBTs	6 MOSFETs	6 MOSFETs
Current stress	High	Low	High
Standalone diodes	16	10	10
Electrolytic capacitors	No	Yes	No
High output current ripple	Yes	No	Yes
Number of magnetic parts	1 transformer with 4 windings	1 transformer with 2 windings 2 PFC inductors	1 transformer with 2 windings 2 buck-boost inductors
Control complexity	Fixed duty ratio and quasi const switching frequency	Duty ratio regulation for PFC Frequency regulation for LLC	Constant frequency for LLC and quasi const duty ratio for Buck-boost
Soft-switching	ZCS for all switches	ZVS for LLC only	ZVS for LLC at higher input voltage, ZCS for buck-boost
Efficiency	High (~93%)	Highest (~95%)	High (~93%)
Reliability and life	Very good	Good	Very good

V. CONCLUSION

In this paper, a 3.3-kW single-stage resonant battery-charger topology has been studied. The PFC has been realized just by keeping the switching frequency constant. By charging the battery with a sinusoidal-like dc current, the input ac power directly transfers to the battery side. Both the bulky PFC inductor and the dc-link capacitor in a traditional two-stage charger are eliminated. All the power switches are turned on and off at a ZCS condition; thus, the efficiency is improved. The presented topology realizes high efficiency, compact size, easy control, and no need for electrolytic capacitor at the same time, which are particularly suitable for the onboard charging applications in the EV and the PHEV. The guidelines that have been presented in this paper can guide the design of such chargers with minimal effort.

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