

# A Novel Soft-Switching Bidirectional DC–DC Converter With Coupled Inductors

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**Abstract**—This paper presents a novel topology for a nonisolated bidirectional dc–dc converter with soft-switching capabilities, which usually operates at a zero-voltage-switching (ZVS) condition. A nonisolated dc–dc converter combines a buck converter and a backward boost converter into one circuit, which consists of a half-bridge power switch, an inductor, and capacitors. In order to realize ZVS conditions, the proposed converter utilizes a coupled inductor, a small independent inductor, and auxiliary switches and diodes. Due to ZVS, switching stress on switch components is reduced, and the reverse recovery problem of MOSFET antiparallel body diodes is also eliminated. Moreover, the operating modes of the proposed converter can be switched between a ZVS mode and a conventional hard-switching mode on the basis of load conditions. The soft-switching mode is for heavy loads, and the hard-switching mode is for light-load conditions. Therefore, the highest efficiency can be obtained at almost all load ranges. The detailed theoretical analyses in each mode are presented, and a 1-kW prototype is also built to verify the principle of the circuit and the theoretical analysis.

**Index Terms**—Bidirectional, coupled inductor, dc–dc converter, resonant power converter, zero-voltage switching (ZVS).

## I. INTRODUCTION

**B**IDIRECTIONAL dc–dc converters can deliver energy between dc sources or loads in either direction. They have been widely used in various areas, such as appliances, general industries, and aerospace, which include uninterruptible power supplies, intelligent battery chargers, hybrid energy storage systems (HESSs) for electric vehicles (EVs) and hybrid EVs, power converters for fuel cell vehicles, and solar power supplies for satellites [1]–[13]. In a HESS [11]–[13], a bidirectional dc–dc converter can be used to match different energy storage systems with different voltage levels, such as batteries and

ultracapacitors, which can supply large bursts of power during start-up, acceleration, and hill climbing, and also recapture a large amount of energy during regenerative braking. Small size and high efficiency are the basic requirements for these types of converters. In order to reduce the converter size, high-switching-frequency operation is needed. However, the total efficiency will significantly drop as the switching losses increase with switching frequency. Hence, soft-switching techniques are usually adopted to reduce switching losses. The use of soft switching can also decrease voltage and current stresses on power switching components and increase the reliabilities of dc–dc converters.

Usually, bidirectional dc–dc converters can be divided into nonisolated types and isolated types, depending on isolation requirements and voltage transfer ratios. This paper mainly focuses on nonisolated bidirectional dc–dc converters, which usually adopt the combination of a buck converter and a backward boost converter in a half-bridge configuration [14]. Some nonisolated bidirectional soft-switching topologies have been proposed in the literature and can be roughly classified into three types.

- 1) Utilizing auxiliary inductors, switches, and capacitors [15]–[19]. By generating resonance between inductors and capacitors, a zero-voltage condition or a zero-current condition is realized. However, higher voltage stress and current stress on switches are also generated. Auxiliary switches usually operate under hard-switching conditions [15], [16] and are switched twice in a switching circle [18]. Thus, switching losses increase, and the control mechanisms become very complicated. In [19], two independent auxiliary circuits are used to implement the soft switching for buck mode and boost mode, respectively. Therefore, it will result in high costs and complexities.
- 2) Adopting the interleaved structure [20]–[23]. Several conventional bidirectional dc–dc converters are connected in parallel to constitute interleaved structures [20]. To achieve zero-voltage-switching (ZVS) conditions, inductor currents flow in bidirectional directions (positive and negative), and the negative inductor current is used to charge and discharge the snubber capacitors. Since the current ripple in each phase is large, multiphase interleaved structures can be used to reduce the summed current ripple. In addition, two phase inductors are coupled with the same magnetic core to reduce the inductor current ripple in each phase, and it can also reduce the iron core losses, size, and cost of converters [21]. In this

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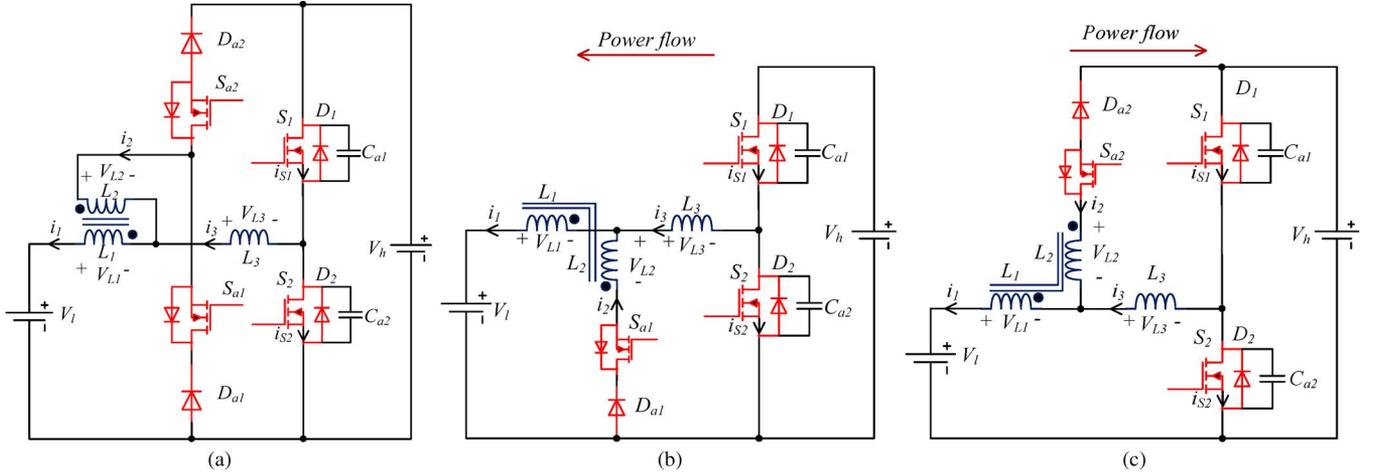


Fig. 1. Proposed ZVS bidirectional dc/dc topology. (a) Complete topology. (b) Simplified topology of buck mode. (c) Simplified topology of boost mode.

method, there are many components such as switches and inductors in multiphase interleaved structures, and the control algorithm is complex.

- 3) Using coupled inductors [24]–[28]. By adding an auxiliary winding with the main inductor, it can supply another power flow channel to achieve soft-switching conditions. In [24], its current ripple can be zero regardless the direction of power flow. It is very beneficial to the battery as the low side voltage source. In [28], a unidirectional ZVS topology with coupled inductor is presented, and the recycled energy is critical for ZVS conditions. However, the drawback of this converter is the recycled energy, which increases as the load decreases. Thus, the efficiency is very low at light conditions.

In this paper, in order to achieve bidirectional capability and improve the efficiency at light-load conditions, a novel nonisolated bidirectional soft-switching dc–dc converter is proposed based on a ZVS converter [28]. The auxiliary circuit consists of a coupled inductor, a small separate inductor, two MOSFETs, and two diodes. The main MOSFETs can operate under ZVS conditions. Two additional MOSFETs are used to determine whether the converter operates at a ZVS mode or a conventional hard-switching mode. One of the two will always turn on or off at buck or boost modes, so there are no switching losses for the two additional MOSFETs. Therefore, the converter can obtain the highest efficiency at both heavy and light loads. A converter prototype rated at 1 kW was built to verify the principles.

The rest of this paper is organized as follows. In Section II, the converter topology and its detailed operating principle of each mode are presented. The design principles of inductors and snubber capacitors are given in Section III. Section IV focuses on the experimental results and analyses. Finally, the conclusion is drawn in Section V.

## II. CONVERTER TOPOLOGY AND OPERATING PRINCIPLE

The proposed ZVS bidirectional dc–dc converter topology as shown in Fig. 1(a) has two distinct operation modes: a buck mode and a boost mode, which are illustrated in Fig. 1(b) and (c), respectively. In this topology, inductors  $L_1$  and  $L_2$  are tightly

coupled on the same ferrite core, and it is assumed that there is no leakage inductance. Due to the existence of  $L_2$ , the current across  $L_3$  is bidirectional (positive and negative), and there is a recycled energy, which is critical for achieving soft switching. In buck mode,  $S_{a2}$  is always off, and  $S_{a1}$  is always on;  $S_1$  and  $S_2$  are the main power switches. In contrast,  $S_{a1}$  is always off, and  $S_{a2}$  is always on in boost mode. The detailed theoretical analyses of steady-state operation in buck and boost modes will be presented in the following sections. In the theoretical analyses, one switching period is divided into seven intervals, and the equivalent circuits for each interval will be also given.

### A. Buck Mode

For the steady-state operation in buck mode, the waveforms of  $i_1$ ,  $i_2$ ,  $i_3$ ,  $V_{GS1}$ ,  $V_{S1}$ ,  $i_{S1}$ ,  $V_{GS2}$ ,  $V_{S2}$ , and  $i_{S2}$  are shown in Fig. 2. The equivalent circuits are shown in Fig. 3, where the red solid arrows denote the actual current directions of each branch in each mode.

*Mode 1* [ $t_0$ – $t_1$ , Fig. 3(a)]: Before  $t_0$ ,  $S_1$  has been triggered to conduct, and  $i_2$  has been decreasing. At  $t_0$ ,  $i_2$  decreases to zero, and  $D_{a1}$  turns off. Then, this mode starts. Currents  $i_3$  and  $i_1$  are equal and increase linearly. This mode is similar to the conventional buck converter. The slopes of  $i_1$ ,  $i_2$ , and  $i_3$  are

$$\frac{di_1}{dt} = \frac{di_3}{dt} = \frac{V_h - V_1}{L_1 + L_3} \quad \frac{di_2}{dt} = 0. \quad (1)$$

*Mode 2* [ $t_1$ – $t_2$ , Fig. 3(b)]: At  $t_1$ ,  $S_1$  turns off, and then, resonance occurs between inductors ( $L_1, L_3$ ) and snubber capacitors ( $C_{a1}, C_{a2}$ ).  $C_{a1}$  is charged, and  $C_{a2}$  is discharged at the same time. When the voltage across  $C_{a2}$  decreases to zero,  $D_2$  will conduct automatically. This interval is very short, so it is assumed that the current in  $L_3$  does not change in this mode. The transition time  $T_{m1}$  can be considered as follows:

$$T_{m1} = t_2 - t_1 = (C_{a1} + C_{a2}) \frac{V_h}{I_{L3\max}} \quad (2)$$

where  $I_{L3\max}$ , the value of  $i_3$  at  $t_1$ , is positive and reaches the maximum in one switching cycle.

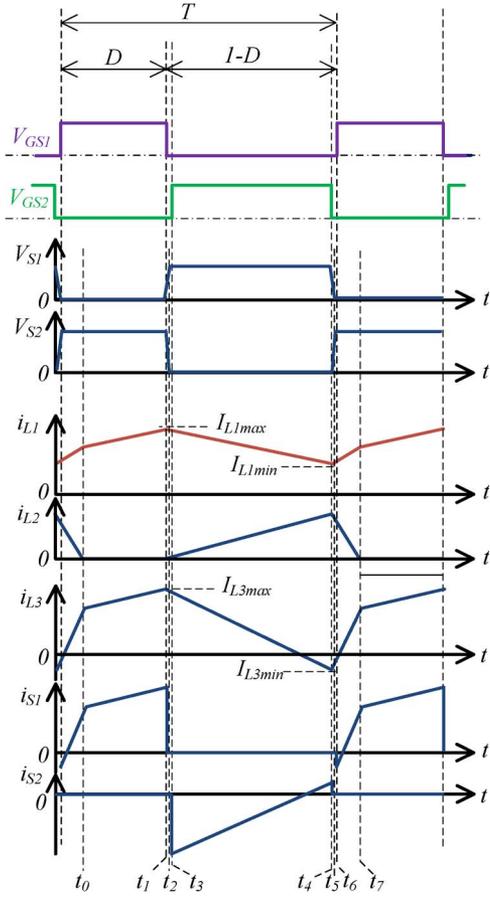


Fig. 2. Waveforms of  $i_1$ ,  $i_2$ ,  $i_3$ ,  $V_{GS1}$ ,  $V_{S1}$ ,  $i_{S1}$ ,  $V_{GS2}$ ,  $V_{S2}$ , and  $i_{S2}$  in buck mode.

*Mode 3* [ $t_2-t_3$ , Fig. 3(c)]: When  $D_2$  conducts,  $D_{a1}$  will conduct at the same time. The following analyses will explain the condition that  $D_{a1}$  will conduct. At first, it is assumed that  $D_{a1}$  does not turn on. Several equations can be obtained as follows:

$$V_{L1} = V_i \times \frac{L_1}{L_1 + L_3}. \quad (3)$$

$L_1$  and  $L_2$  are completely coupled on the same core, and  $n_1$  and  $n_2$  are the turns of  $L_1$  and  $L_2$ , respectively; therefore,

$$\frac{n_2}{n_1} = \sqrt{\frac{L_2}{L_1}}. \quad (4)$$

Thus,

$$V_{L2} = \frac{n_2}{n_1} V_{L1} = \frac{n_2}{n_1} \times V_i \times \frac{L_1}{L_1 + L_3} = \sqrt{\frac{L_2}{L_1}} \times \frac{V_i L_1}{L_1 + L_3}. \quad (5)$$

From the Kirchhoff's voltage law (KVL) equation, we can obtain

$$V_i - V_{L1} - V_{L2} - V_{D_{a1}} = 0. \quad (6)$$

Substituting (3) and (5) to (6), we can obtain

$$V_{D_{a1}} = V_i \times \frac{L_3 - M}{L_1 + L_3} \quad (7)$$

$$M = \sqrt{L_1 L_2} \quad (8)$$

where  $M$  is the mutual inductance between  $L_1$  and  $L_2$ .

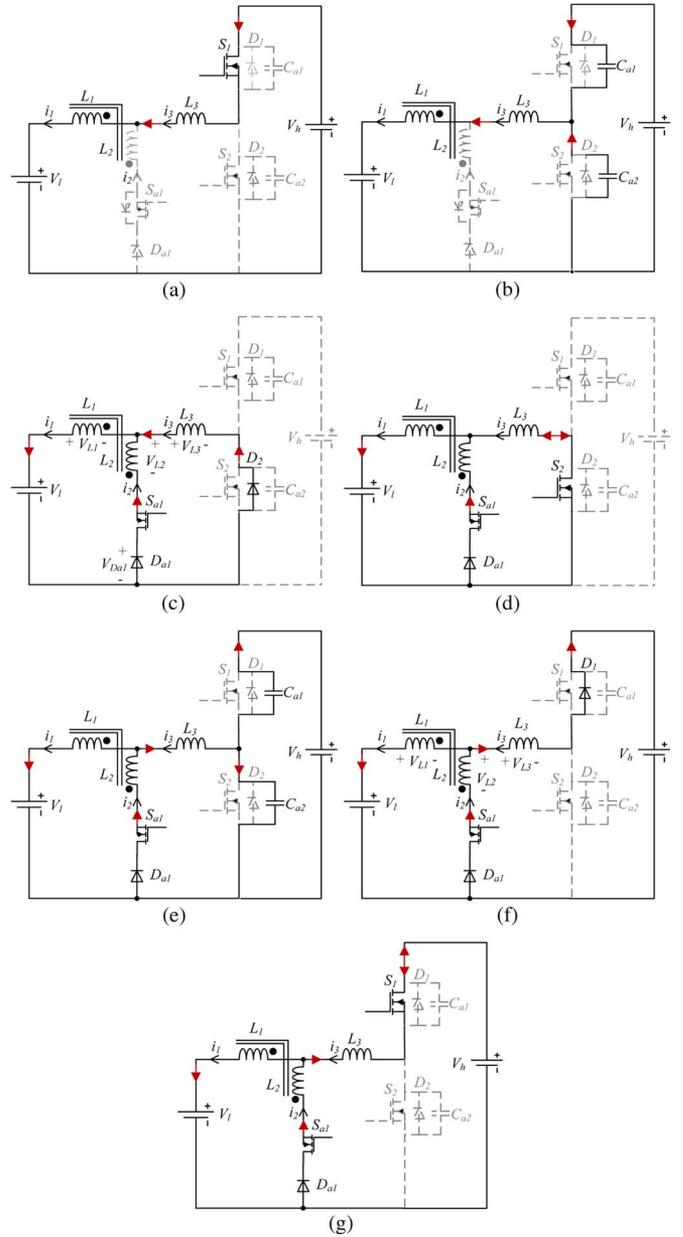


Fig. 3. Equivalent circuits for each operation mode of buck mode. (a) Mode 1,  $t_0-t_1$ . (b) Mode 2,  $t_1-t_2$ . (c) Mode 3,  $t_2-t_3$ . (d) Mode 4,  $t_3-t_4$ . (e) Mode 5,  $t_4-t_5$ . (f) Mode 6,  $t_5-t_6$ . (g) Mode 7,  $t_6-t_7$ .

If  $V_{D_{a1}}$  is less than zero,  $D_{a1}$  will conduct. Therefore, if  $D_{a1}$  will conduct, the next inequality must be satisfied

$$L_3 < M. \quad (9)$$

After  $D_{a1}$  conducts,  $V_{D_{a1}}$  is equal to zero, so the decoupled equivalent circuit of this mode is shown in Fig. 4(a), and the current slopes of  $L_1$ ,  $L_2$ , and  $L_3$  can be derived as shown hereinafter.

Based on KVL and Kirchhoff's current law (KCL), we can obtain

$$\begin{cases} i_1 = i_2 + i_3 \\ V_i - V_{L1+M} - V_{L3-M} = 0 \\ V_{L2+M} - V_{L3-M} = 0. \end{cases} \quad (10)$$

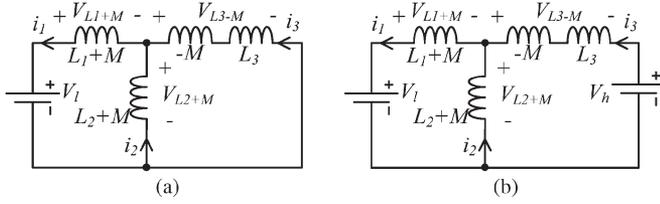


Fig. 4. Decoupled equivalent circuits for buck mode. (a) Modes 3 and 4. (b) Modes 6 and 7.

Then,

$$\begin{cases} \frac{di_1}{dt} = \frac{di_2}{dt} + \frac{di_3}{dt} \\ V_l + (L_1 + M) \frac{di_1}{dt} + (L_3 - M) \frac{di_3}{dt} = 0 \\ -(L_2 + M) \frac{di_2}{dt} + (L_3 - M) \frac{di_3}{dt} = 0. \end{cases} \quad (11)$$

So, the current slopes are obtained as follows:

$$\frac{di_1}{dt} = -\frac{V_l(L_3 + L_2)}{(L_1 + L_2 + 2M)L_3} \quad (12)$$

$$\frac{di_2}{dt} = \frac{V_l(M - L_3)}{(L_1 + L_2 + 2M)L_3} \quad (13)$$

$$\frac{di_3}{dt} = -\frac{V_l(L_2 + M)}{(L_1 + L_2 + 2M)L_3}. \quad (14)$$

Because  $L_3$  is comparatively small,  $i_3$  will decrease much faster than  $i_1$ . As long as  $D_2$  is on,  $S_2$  can be triggered to turn on under ZVS condition. Then, this mode naturally ends. In addition, the total duration time of modes 2 and 3 is equal to the dead time of the triggering pulse signals.

*Mode 4* [ $t_3-t_4$ , Fig. 3(d)]: At  $t_3$ ,  $S_2$  is turned on to carry on the current. The converter comes into the freewheeling stage, in which  $i_3$  decreases from positive to negative. The decoupled equivalent circuit of this mode is identical to that of mode 3, so current slopes are also the same as those of mode 3. When  $S_2$  turns off, this mode ends, and  $i_3$  decreases to its minimum  $I_{L3\min}$ , which is critical for supplying ZVS conditions. The energy stored in  $L_3$  must be large enough to charge and discharge the snubber capacitors fully, so that ZVS condition can be achieved. It can be expressed as

$$\frac{1}{2}L_3I_{L3\min}^2 > \frac{1}{2}(C_{a1} + C_{a2})V_h^2. \quad (15)$$

When the load is the heaviest, the energy stored in  $L_3$  is the least, so the maximum load is the worst situation for achieving ZVS conditions.

*Mode 5* [ $t_4-t_5$ , Fig. 3(e)]: At  $t_4$ ,  $S_2$  turns off, and then, snubber capacitor  $C_{a1}$  is discharged and  $C_{a2}$  is charged. When the voltage across  $C_{a1}$  reduces to zero,  $D_1$  will conduct automatically. It provides ZVS conditions for  $S_1$  turn-on. The transition time  $T_{m5}$  is also very short, and it can be assumed that  $i_3$  is constant in this mode.  $T_{m5}$  can be obtained as follows:

$$T_{m5} = t_5 - t_4 = (C_{r1} + C_{r2}) \frac{V_b}{|I_{L3\min}|} \quad (16)$$

where  $I_{L3\min}$  is the real value of  $i_3$  at  $t_4$  and also the minimum. The heavier the load is, the longer  $T_{m5}$  is. At the maximum load,  $T_{m5}$  has reached the maximum, which must be less than

the dead time of the gate trigger signals. Otherwise, if  $T_{m5}$  is larger than the dead time, ZVS will not be achieved.

*Mode 6* [ $t_5-t_6$ , Fig. 3(f)]: When  $D_1$  conducts,  $i_3$  and  $i_1$  begin to increase, and  $i_2$  decreases. Conduction of  $D_1$  provides a ZVS condition for  $S_1$  to be turned on. After  $D_1$  conducts,  $S_1$  can be turned on immediately, and then, this mode is ended. In addition, the total duration time of modes 5 and 6 is also equal to the dead time of the triggering pulse signals. The decoupling equivalent circuit of this mode is shown in Fig. 4(b), and the slopes of the three inductor currents can be derived as follows.

Based on KVL and KCL, we can obtain

$$\begin{cases} i_1 = i_2 + i_3 \\ V_l - V_{L1+M} - V_{L2+M} = 0 \\ V_{L2+M} - V_{L3-M} - V_h = 0. \end{cases} \quad (17)$$

Then,

$$\begin{cases} \frac{di_1}{dt} = \frac{di_2}{dt} + \frac{di_3}{dt} \\ V_l + (L_1 + M) \frac{di_1}{dt} + (L_2 + M) \frac{di_2}{dt} = 0 \\ -(L_2 + M) \frac{di_2}{dt} + (L_3 - M) \frac{di_3}{dt} - V_h = 0. \end{cases} \quad (18)$$

So, the current slopes are obtained as follows:

$$\frac{di_1}{dt} = \frac{V_h L_2}{(L_2 + M)L_3} - \frac{V_l(L_3 + L_2)}{(L_1 + L_2 + 2M)L_3} \quad (19)$$

$$\frac{di_2}{dt} = -\frac{V_h L_1}{(L_1 + M)L_3} + \frac{V_l(M - L_3)}{(L_1 + L_2 + 2M)L_3} \quad (20)$$

$$\frac{di_3}{dt} = \frac{V_h}{L_3} - \frac{V_l(L_2 + M)}{(L_1 + L_2 + 2M)L_3}. \quad (21)$$

*Mode 7* [ $t_6-t_7$ , Fig. 3(g)]: At  $t_6$ ,  $S_1$  is triggered on. Current  $i_3$  continues to increase from negative to positive, and  $i_1$  also increases. Finally,  $i_1$  and  $i_3$  will be equal at  $t_7$ , so that  $i_2$  becomes zero and  $D_1$  turns off; then, this mode ends, and the converter enters into mode 1 as the beginning of the next switching period.

Since the decoupled equivalent circuit is the same as that of mode 6, the current slopes of this mode are identical to those of mode 6, so the derivation process is omitted.

## B. Boost Mode

For the steady-state operation in boost mode,  $S_{a1}$  is always off, and  $S_{a2}$  is always on. Waveforms of  $i_1$ ,  $i_2$ ,  $i_3$ ,  $V_{GS1}$ ,  $V_{S1}$ ,  $i_{S1}$ ,  $V_{GS2}$ ,  $V_{S2}$ , and  $i_{S2}$  in boost mode, as shown in Fig. 5, are similar to those in buck mode, but the directions are opposite. The converter also has seven distinct operating modes in a switching cycle. The equivalent circuit for each operation mode is shown in Fig. 6.

*Mode 1* [ $t_0-t_1$ , Fig. 6(a)]: Before  $t_0$ ,  $S_2$  has been conducting, and  $i_2$  has been increasing. At  $t_0$ ,  $i_2$  increases to zero, and  $D_{a2}$  turns off; then, this mode starts. Currents  $i_3$  and  $i_1$  are identical and decrease linearly until  $S_2$  turns off. This mode is also similar to that of conventional boost converters. The slopes of  $i_1$ ,  $i_2$ , and  $i_3$  are

$$\frac{di_1}{dt} = \frac{di_3}{dt} = \frac{-V_l}{L_1 + L_3} \quad \frac{di_2}{dt} = 0. \quad (22)$$

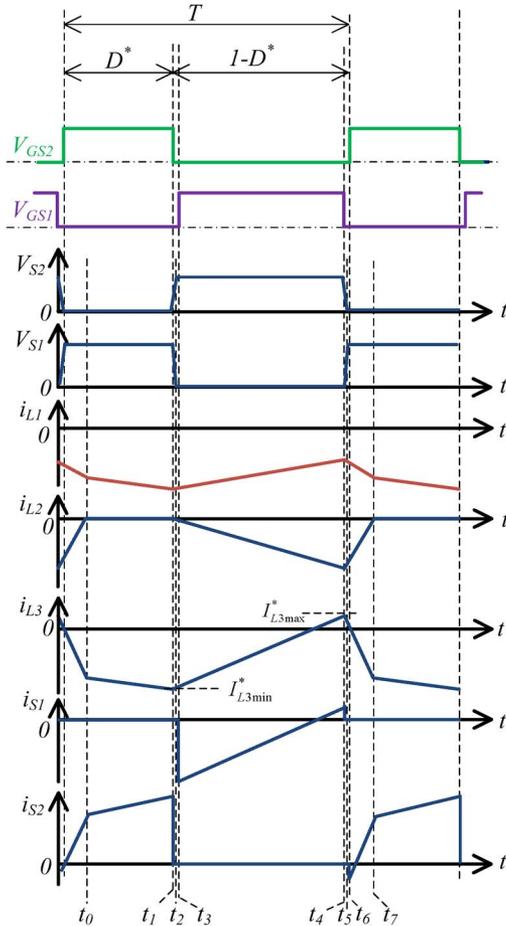


Fig. 5. Waveforms of  $i_1$ ,  $i_2$ , and  $i_3$  in boost mode.

*Mode 2* [ $t_1-t_2$ , Fig. 6(b)]: At  $t_1$ ,  $S_2$  turns off, and then, a resonance starts between the inductor ( $L_3$ ) and snubber capacitors ( $C_{a1}$  and  $C_{a2}$ ).  $C_{a1}$  is discharged, and  $C_{a2}$  is charged at the same time. When the voltage across  $C_{a1}$  decreases to zero,  $D_1$  will conduct automatically. As this duration is very short, it can be supposed that  $i_3$  would not change. The duration time  $T_{m1}^*$  can be obtained as follows:

$$T_{m1}^* = t_2 - t_1 = (C_{r1} + C_{r2}) \frac{V_h}{|I_{L3max}^*|} \quad (23)$$

where  $I_{L3max}^*$  is the value of  $i_3$  at  $t_1$ , and its absolute value is the greatest in a whole switching period. Usually, the energy stored in  $L_3$  is enough to charge and discharge the auxiliary capacitors.

*Mode 3* [ $t_2-t_3$ , Fig. 6(c)]: When  $D_1$  conducts,  $D_{a2}$  will conduct at the same time, the reason of which can be obtained by the same method used in mode 3 of buck mode. Then, it can also be obtained that the condition is the same as that of buck mode, i.e., inequality (9) must be satisfied. After  $D_1$  conducts, the voltage across  $S_1$  is zero, so  $S_1$  can be turned on under ZVS condition. The decoupling equivalent circuit is shown in Fig. 7(a), and the current slopes of inductors  $L_1$ ,  $L_2$ , and  $L_3$  can be derived as shown hereinafter.

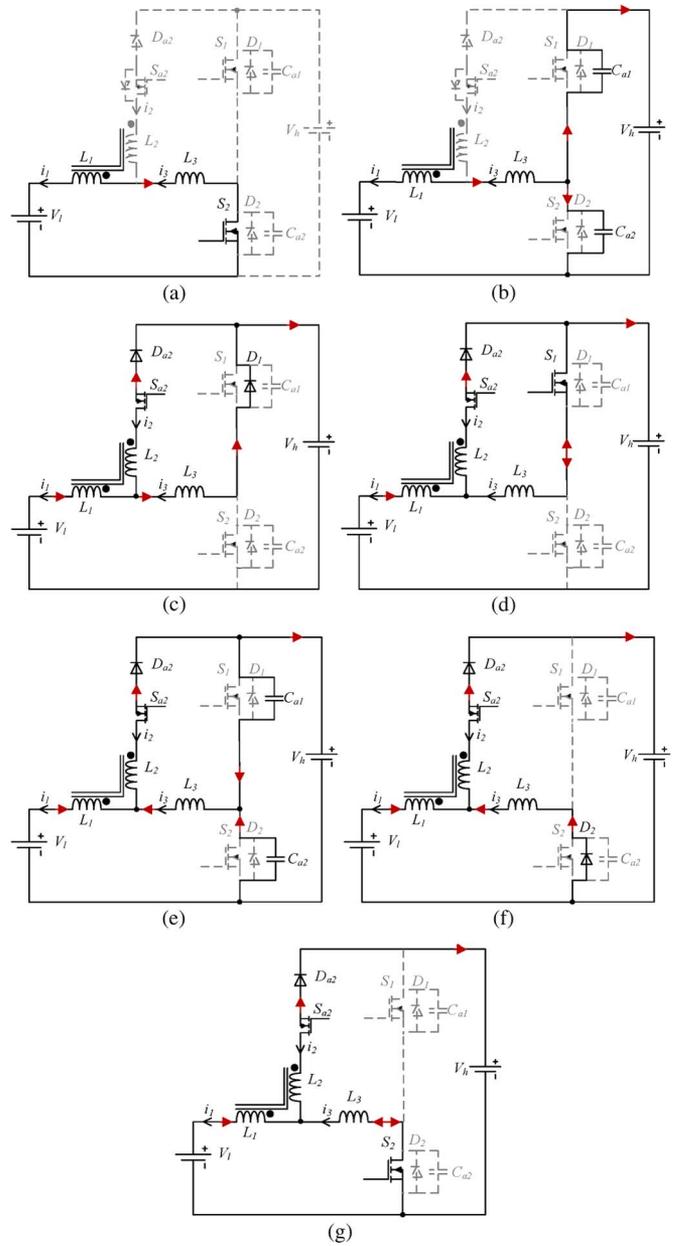


Fig. 6. Equivalent circuits for each operation mode of boost mode. (a) Mode 1,  $t_0-t_1$ . (b) Mode 2,  $t_1-t_2$ . (c) Mode 3,  $t_2-t_3$ . (d) Mode 4,  $t_3-t_4$ . (e) Mode 5,  $t_4-t_5$ . (f) Mode 6,  $t_5-t_6$ . (g) Mode 7,  $t_6-t_7$ .

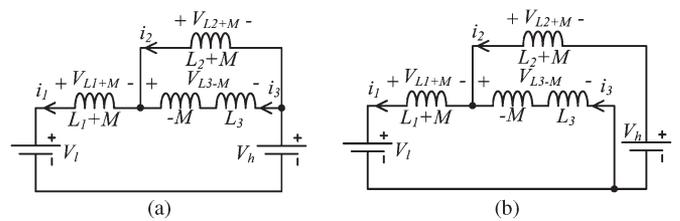


Fig. 7. Decoupled equivalent circuits for boost mode. (a) Modes 3 and 4. (b) Modes 6 and 7.

Based on KVL and KCL, we can obtain

$$\begin{cases} i_1 = i_2 + i_3 \\ V_l - V_{L1+M} - V_{L2+M} - V_h = 0 \\ V_{L2+M} - V_{L3-M} = 0. \end{cases} \quad (24)$$

Then,

$$\begin{cases} \frac{di_1}{dt} = \frac{di_2}{dt} + \frac{di_3}{dt} \\ V_l + (L_1 + M) \frac{di_1}{dt} + (L_2 + M) \frac{di_2}{dt} - V_h = 0 \\ -(L_2 + M) \frac{di_2}{dt} + (L_3 - M) \frac{di_3}{dt} = 0. \end{cases} \quad (25)$$

So, the current slopes are obtained as

$$\frac{di_1}{dt} = \frac{(V_h - V_l)(L_3 + L_2)}{(L_1 + L_2 + 2M)L_3} \quad (26)$$

$$\frac{di_2}{dt} = -\frac{(V_h - V_l)(M - L_3)}{(L_1 + L_2 + 2M)L_3} \quad (27)$$

$$\frac{di_3}{dt} = \frac{(V_h - V_l)(L_2 + M)}{(L_1 + L_2 + 2M)L_3}. \quad (28)$$

Based on (26)–(28), since  $L_3$  is very small, it can be easily seen that  $i_3$  increases faster than  $i_1$ , and  $i_2$  increases in the negative direction. When  $S_1$  is triggered on,  $D_1$  naturally turns off, and this mode ends. The total duration time of modes 2 and 3 is equal to the dead time of triggering pulse signals.

*Mode 4* [ $t_3$ – $t_4$ , Fig. 6(d)]: At  $t_3$ ,  $S_1$  turns on, and  $i_3$  continues to increase from negative to positive across  $S_1$ .  $S_1$  will be turned off until  $i_3$  goes up to its maximum  $I_{L3\max}^*$  at  $t_4$ .  $I_{L3\max}^*$  must be large enough to make sure that the energy stored in  $L_3$  can thoroughly charge  $C_{a1}$  and discharge  $C_{a2}$ . When the load is the heaviest, the energy stored in  $L_3$  is the least, so the maximum load is the worst situation for ZVS in boost mode

$$\frac{1}{2}L_3 I_{L3\max}^{*2} > \frac{1}{2}(C_{r1} + C_{r2})V_h^2. \quad (29)$$

When  $S_1$  turns off, this mode is over. In addition, the decoupled equivalent circuit and the slopes of  $i_1$ ,  $i_2$ , and  $i_3$  are the same to those of mode 3.

*Mode 5* [ $t_4$ – $t_5$ , Fig. 6(e)]: After  $S_1$  is off at  $t_4$ , resonance begins.  $C_{a1}$  is charged, and  $C_{a2}$  is discharged. Then, the voltage across  $S_2$  decreases to zero, which supplies ZVS conditions for  $S_2$  turn-on. The duration time of this mode is very short and can be calculated as follows:

$$T_{m5}^* = t_5 - t_4 = (C_{a1} + C_{a2}) \frac{V_h}{I_{L3\max}^*}. \quad (30)$$

It must be smaller than the dead time of the gate drive signals. Otherwise, ZVS cannot be achieved. When the voltage across  $S_2$  decreases to zero,  $D_2$  automatically turns on, and this mode is ended.

*Mode 6* [ $t_5$ – $t_6$ , Fig. 6(f)]: Conduction of  $D_2$  provides ZVS condition for  $S_2$  to be turned on at  $t_5$ . The decoupled equivalent circuit is shown in Fig. 7(b). Based on KVL and KCL, some equations are obtained, and three current slopes are derived.

$$\begin{cases} i_1 = i_2 + i_3 \\ V_l - V_{L1+M} - V_{L3-M} = 0 \\ V_{L3-M} - V_{L2+M} - V_h = 0. \end{cases} \quad (31)$$

Then,

$$\begin{cases} \frac{di_1}{dt} = \frac{di_2}{dt} + \frac{di_3}{dt} \\ V_l + (L_1 + M) \frac{di_1}{dt} + (L_3 - M) \frac{di_3}{dt} = 0 \\ -(L_3 - M) \frac{di_3}{dt} + (L_2 + M) \frac{di_2}{dt} - V_h = 0. \end{cases} \quad (32)$$

So, the current slopes are as follows:

$$\frac{di_1}{dt} = -\frac{V_l(L_2 + L_3)}{(L_1 + L_2 + 2M)L_3} - \frac{V_h(M - L_3)}{(L_1 + L_2 + 2M)L_3} \quad (33)$$

$$\frac{di_2}{dt} = \frac{V_l(M - L_3)}{(L_1 + L_2 + 2M)L_3} + \frac{V_h(L_1 + L_3)}{(L_1 + L_2 + 2M)L_3} \quad (34)$$

$$\frac{di_3}{dt} = -\frac{V_l L_2}{(L_2 + M)L_3} - \frac{V_h L_1}{(L_1 + M)L_3}. \quad (35)$$

*Mode 7* [ $t_6$ – $t_7$ , Fig. 6(g)]: At  $t_6$ ,  $S_2$  is turned on, and then,  $i_3$  continues to decrease across  $S_2$ . Currents  $i_1$  and  $i_3$  will be equal at  $t_7$ , so that  $i_2$  becomes zero, and  $D_{a2}$  naturally turns off. Then, the converter comes into mode 1 as the beginning of the next switching cycle. The decoupled equivalent circuit, as shown in Fig. 7(b), is the same as that of mode 3, so current slopes are also the same.

### III. DESIGN OF INDUCTORS AND SNUBBER CAPACITORS

In this topology, component parameters must be designed properly to ensure that the converter operates under a ZVS condition. The design methods of inductors ( $L_1$ ,  $L_2$ , and  $L_3$ ) and snubber capacitors ( $C_{a1}$  and  $C_{a2}$ ) are analyzed hereinafter. From the analyses of buck mode, it is known that modes 3 and 4 are the current freewheeling stage, in which current slopes remain constant. So, we can use these current slopes and other constraints to calculate the parameters of inductors and capacitors. The freewheeling stage starts at  $t_2$  and ends at  $t_4$ , as shown in Fig. 2. The equivalent circuits are shown in Fig. 3(c) and (d), respectively. Since the maximum load is the worst condition for ZVS conditions, the parameters are designed at the maximum load.

In boost mode, the calculating method is similar to that of buck mode, and if the external conditions are the same, the obtained parameters are also identical. Therefore, only the derivations of parameters in buck mode are given. There are five steps, as discussed in the following.

*Step 1—Duty Ratio*: The relationships of input voltage and output voltage are the same to those of conventional buck and boost converters. Because  $V_h$  and  $V_l$  are known, the duty ratio  $D$  is obtained. It is assumed that the switching frequency is  $f_{sw}$ . So, the freewheeling time can be obtained as

$$\Delta t = \frac{1 - D}{f_{sw}} = \left(1 - \frac{V_l}{V_h}\right) \frac{1}{f_{sw}}. \quad (36)$$

*Step 2—Parameters  $i_1$* : In buck mode, the average of  $i_1$  is equal to the load current. It is supposed that the maximum load current is  $I_{load\max}$ , so the average current of  $L_1$  is equal to  $I_{load\max}$ . The ripple coefficient  $r_{L1}$  of  $i_1$  is usually set as 40% of the average current, so the variation of  $i_1$  with the maximum load in freewheeling stage can be

$$\Delta I_{L1} = I_{L1\min} - I_{L1\max} = -I_{load\max} \times r_{L1}. \quad (37)$$

*Step 3—Parameters  $i_3$* :  $L_3$  is very critical to achieve ZVS, and  $i_3$  decreases from the maximum  $I_{L3\max}$  (positive, equal to  $I_{L1\max}$ ) to the minimum  $I_{L3\min}$  (negative) in the freewheeling

stage. Usually, for achieving ZVS,  $I_{L3\min}$  is as small as possible to supply more energy for charging and discharging the snubber capacitors. However, when the load current is zero, the absolute value of  $I_{L3\min}$  reaches its maximum, which should not be more than  $I_{L3\max}$  because of the limitations of wire size and magnetic saturation. Therefore,  $I_{L3\min}$  at the maximum load is equal to  $-I_{\text{load max}} \times (r_{L1}/2)$ . The variation of  $i_3$  in the freewheeling stage is

$$\Delta I_{L3} = I_{L3\min} - I_{L3\max} = -I_{\text{load max}} \times (1 + r_{L1}). \quad (38)$$

*Step 4—Snubber Capacitor and  $L_3$ :* To achieve ZVS conditions, inequality (15) must be satisfied. In addition, based on the analyses in mode 5, the duration time  $T_{m5}$  is set as 100 ns in this topology. Usually,  $C_{a1}$  and  $C_{a2}$  are the same, and the maximum  $C_{a\max}$  can be obtained. In fact, the selected  $C_{a1}$  and  $C_{a2}$  are smaller than  $C_{a\max}$ , since the effective output capacitance of MOSFET should be included in  $C_{a\max}$ . The derivation processes are as follows:

$$T_{m5} = t_5 - t_4 = (C_{a1} + C_{a2}) \frac{V_h}{|I_{L3\min}|} \leq 100 \text{ ns}. \quad (39)$$

So,

$$C_{a\max} = \frac{50 \times |I_{L3\min}|}{V_h} \text{ pF}. \quad (40)$$

Substituting (40) into (15),

$$L_3 > L_{3\min} = \frac{2C_{a\max}V_h^2}{I_{L3\min}^2} = \frac{V_h}{10 \times |I_{L3\min}|} \text{ uH}. \quad (41)$$

*Step 5— $L_1$  and  $L_2$ :* From (12) and (14), current variations of  $L_1$  and  $L_3$  in the freewheeling stage are expressed as follows:

$$\Delta I_1 = \frac{-V_l(L_3 + L_2)}{(L_1 + L_2 + 2M)L_3} * \Delta t \quad (42)$$

$$\Delta I_3 = \frac{-V_l(L_2 + M)}{(L_1 + L_2 + 2M)L_3} * \Delta t \quad (43)$$

where  $M = \sqrt{L_1 L_2}$ .  $V_l$ ,  $L_3$ ,  $\Delta t$ ,  $\Delta I_1$ , and  $\Delta I_3$  are already known from the four steps mentioned previously, and  $L_1$  and  $L_2$  are obtained by solving (42) and (43). In addition, inequality (9) should be used to verify the solved results of  $L_1$  and  $L_2$ .

#### IV. EXPERIMENT RESULTS

To verify the aforementioned analyses, a prototype converter (1 kW,  $V_h = 100$  V, and  $V_l = 50$  V) has been built. The details of the experimental setup of the proposed converter are presented in Table I. Fig. 8 shows the photograph of the proposed converter prototype. The switching waveforms of  $S_1$  and  $S_2$  are measured to validate ZVS effects. Efficiencies are also measured. In all experiments, both  $i_{S1}$  and  $i_{S2}$  are measured by an ac current measurement probe, because the dc probe cannot be installed on the MOSFETs (package: TO-247). The real zero positions will be marked in each figure.

TABLE I  
EXPERIMENTAL CONDITIONS AND CIRCUIT PARAMETERS

Parameters	Values
$V_h$	100 V
$V_l$	50 V
$f_{sw}$	50 kHz
Maximum output power	1000 W
$L_1$ (turns)	80.7 uH (18)
$L_2$ (turns)	0.78 uH (2)
$L_3$ (turns)	1.3 uH (4)
$C_{a1}, C_{a2}$	3000 pF
MOSFETs	IPW60R041C6
Diodes	60EPU02PbF

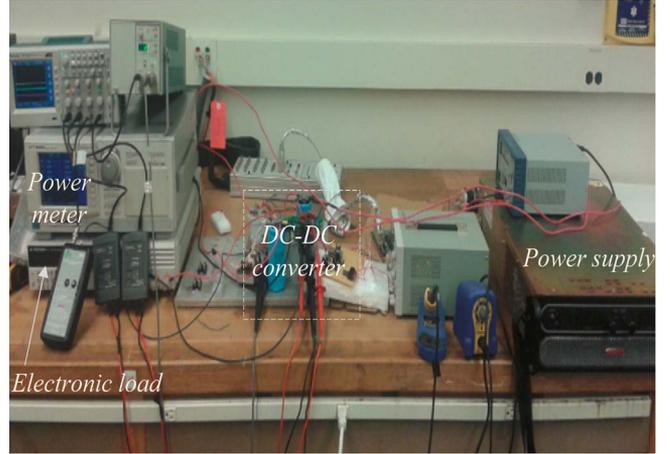


Fig. 8. Experimental setup of the proposed converter.

##### A. Buck Mode

The turn-on process of  $S_1$  is shown in Fig. 9(a). Voltage  $V_{S1}$  across  $S_1$  decreases to zero before the gate trigger signal  $V_{GS1}$  is applied. Therefore, ZVS turn-on is achieved. Fig. 9(b) shows the turnoff process of  $S_1$ . It can be seen that, when the turnoff trigger signal is applied,  $i_{S1}$  decreases sharply to zero, and then,  $V_{S1}$  increases to  $V_h$ . Hence, ZVS is also achieved in the turnoff process.

Fig. 10(a) shows the turn-on process of  $S_2$ . It can be seen that ZVS is achieved at the turn-on process because  $V_{S2}$  has been decreased to zero before the turn-on trigger signal  $V_{GS2}$  starts. The turnoff process of  $S_2$  is shown in Fig. 10(b), where ZVS is also achieved.

##### B. Boost Mode

The turn-on and turnoff processes in boost mode are shown in Fig. 11(a) and (b), respectively. In Fig. 11(a),  $V_{S1}$  reduces to zero before the gate trigger signal  $V_{GS1}$  is applied, so ZVS turn-on is achieved. In Fig. 11(b), when the turnoff trigger signal is applied,  $i_{S1}$  decreases sharply to zero, and then,  $V_{S1}$  increases to  $V_h$ . Therefore, ZVS is also achieved in the turnoff process.

Fig. 12(a) shows the turn-on process of  $S_2$ , in which ZVS is achieved. Fig. 12(b) shows the turnoff process of  $S_2$ , and ZVS is also validated.

From the aforementioned experimental analyses, even at the maximum load, both  $S_1$  and  $S_2$  have realized ZVS turn-on and ZVS turnoff, no matter the converter works in buck mode or boost mode. It can also be shown that both  $S_1$  and  $S_2$

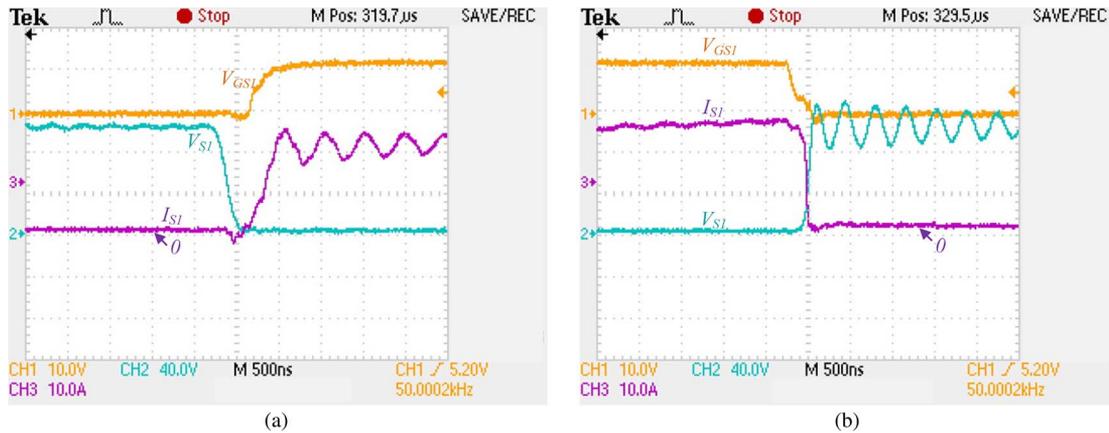


Fig. 9.  $S_1$  switching waveforms in buck mode. (a) Turn-on process. (b) Turnoff process.

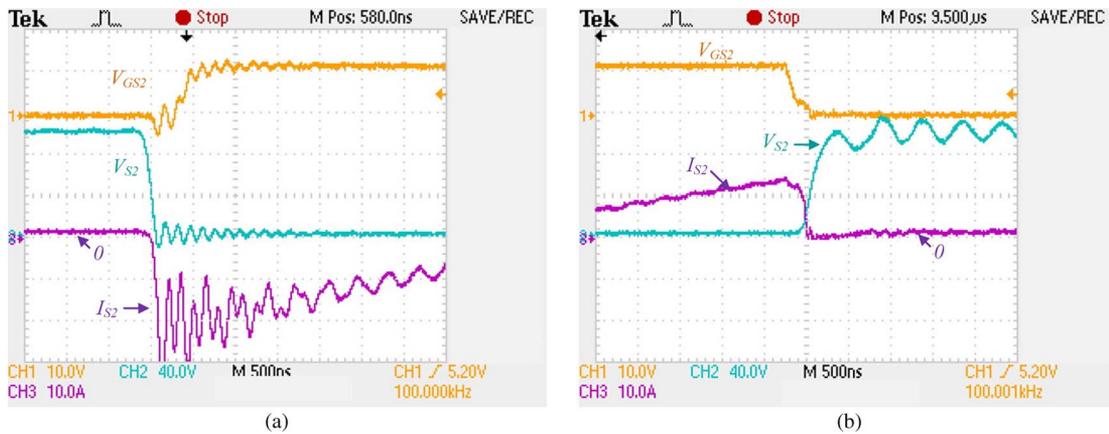


Fig. 10.  $S_2$  switching waveforms in buck mode. (a) Turn-on process. (b) Turnoff process.

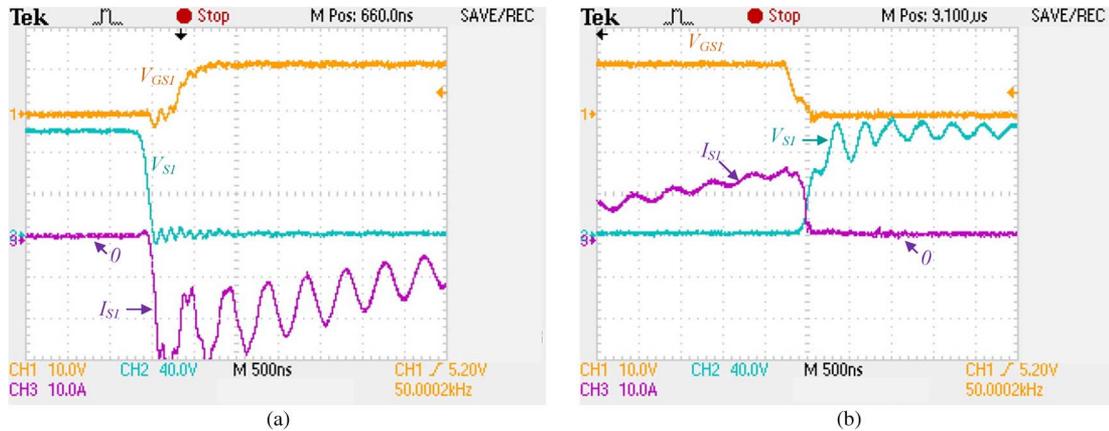


Fig. 11.  $S_1$  switching waveforms in boost mode. (a) Turn-on process. (b) Turnoff process.

operate under ZVS conditions across all load ranges, because the maximum load is the worst case for ZVS. Moreover, it can be seen that the switching waveforms of  $S_1$  in buck mode are similar to those of  $S_2$  in boost mode at the same output power. The switching waveforms of  $S_2$  in buck mode are also similar to those of  $S_1$  in boost mode.

### C. Efficiency Analyses

The efficiency curves in buck mode and boost mode are shown in Fig. 13(a) and (b), respectively. The efficiencies are

measured without regard to the controlling and driving circuits. In each figure, one is measured under the soft-switching mode, and the other is measured under the hard-switching mode as comparison. In hard-switching mode,  $S_{a1}$  and  $S_{a2}$  are always off, and only  $S_1$  and  $S_2$  are controlled by the pulsewidth-modulation controller. Due to soft switching, the proposed converter's efficiencies of buck mode and boost mode are significantly improved at heavy-load conditions, compared with conventional hard-switching mode. However, the efficiencies at light-load conditions under soft switching are not as high as those under the conventional hard-switching mode. It is because

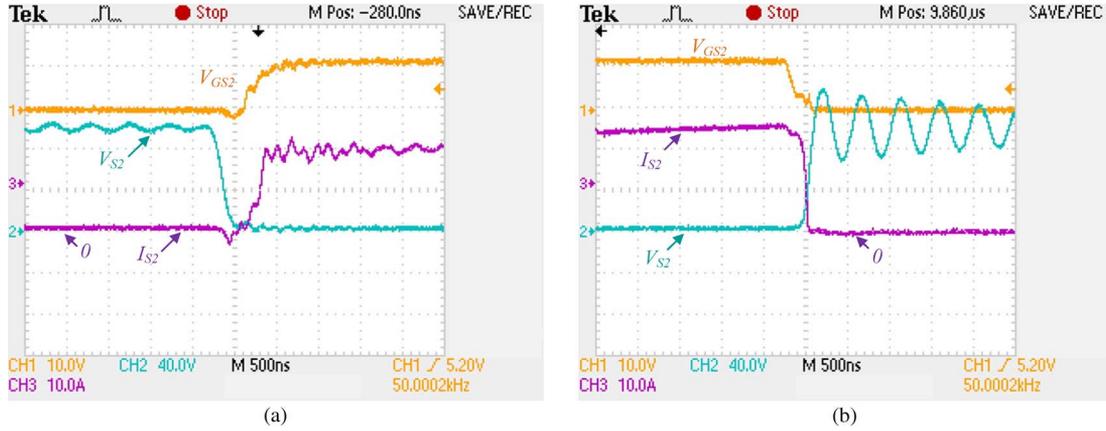


Fig. 12.  $S_2$  switching waveforms in boost mode. (a) Turn-on process. (b) Turnoff process.

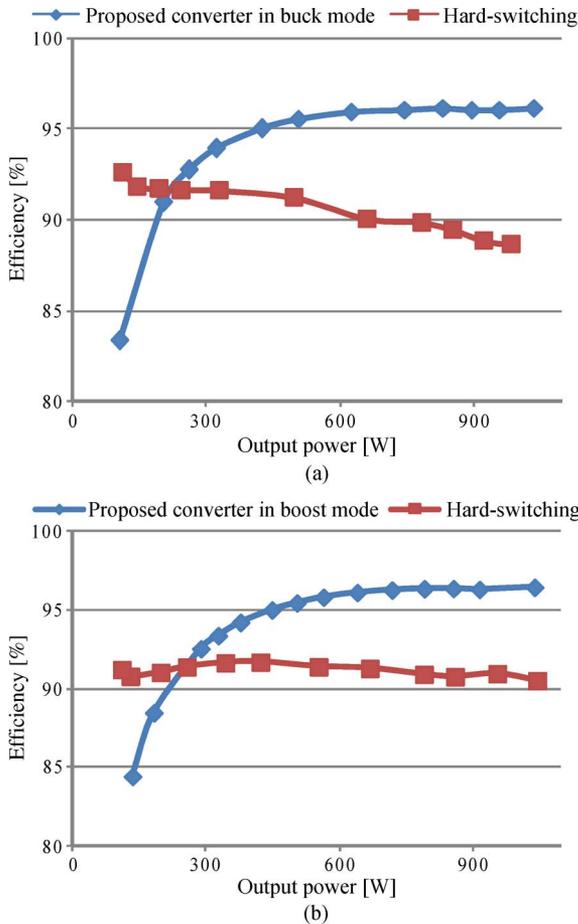


Fig. 13. Measured efficiencies of the proposed converter. (a) Buck mode. (b) Boost mode.

that the recycled energy results in the additional conduction losses of auxiliary circuits.

In Fig. 14, the waveforms of  $i_3$  at different output powers (1035, 617, 320, and 0 W) are shown. It can be seen that, the smaller the output power is, the bigger the absolute value of  $i_3$  minimum is, i.e., the greater the recycled energy is. Thus, it will result in more conduction losses at a lower output power. In addition, the varying trends of each waveform are similar, and the peak-to-peak values are almost equal, which is equal

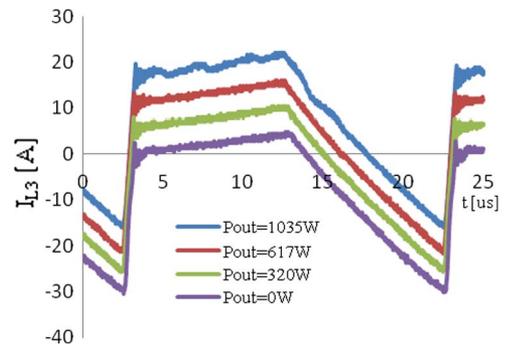


Fig. 14.  $i_{L3}$  waveforms at different output powers in buck mode.

to the maximum of  $i_2$ . It means that the maximum of  $i_2$  is the same at all load conditions, so the conduction loss of the branch circuit of  $L_2$  always exists and remains a constant regardless of the load condition. Therefore, for the proposed converter, the efficiency of the conventional hard-switching mode at a light load is higher than that of the soft-switching mode. In order to always obtain higher efficiency and alleviate the effect of the recycled energy, its operating mode of the proposed converter can be switched between the hard- and soft-switching modes. When the load is heavy, it works under the soft-switching mode, and when the load is light, it works under the conventional hard-switching mode.

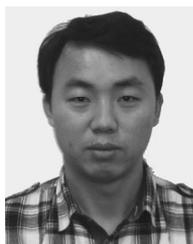
### V. CONCLUSION

In this paper, a novel nonisolated bidirectional soft-switching dc-dc converter has been proposed. In buck and boost modes, the power MOSFETs can operate under ZVS conditions. The detailed operating principles in each mode have been presented, and the design steps of the main circuit have also been discussed. The prototype of the proposed converter was built, and the experiment results verify that ZVS is achieved and other theoretical analyses are correct. Compared with hard-switching mode, efficiencies are improved, with up to 96.46% in boost mode and 96.03% in buck mode at the maximum load. Moreover, in order to avoid the impact of the large recycled energy at light-load conditions, the change between hard- and

soft-switching modes can be utilized to obtain high efficiencies at light-load conditions.

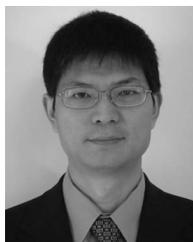
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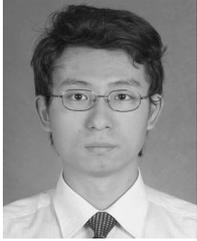
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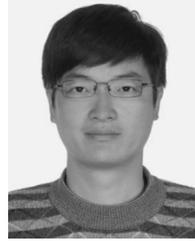
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