Framework and Research Methodology of Short-Timescale Pulsed Power Phenomena in High-Voltage and High-Power Converters

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***Abstract*—Various short-timescale transients exist in power electronic converters, particularly in high-voltage and high-power systems. The timescales of these transients are from nanoseconds to microseconds, including a switching transition of power semiconductor devices, commutating processes, and drive signal transmissions. These transient processes directly affect the performance and reliability of power electronic systems. Therefore, it is necessary to study these short-timescale processes. Based on two high-power prototype power converters, a 6000-V/1250-kW three-level adjustable-speed drive and a 10-kW/600-V dc–dc converter, this paper studies the various abnormal behaviors of the converters that occurred during the operation of these converters. Dead bands and accumulated switching errors are also investigated. A combined microscopic pulsed power and macroscopic control strategy was proposed for the design of power electronic converters. Three new concepts for power electronic converters are introduced and validated in this paper: 1) sneak pulse; 2) energy dead band; and 3) transient commutating topology.**

***Index Terms*—Adjustable-speed drive (ASD), dc–ac inverter, dc–dc converter, dead band, isolation, minimum pulsewidth, phase-shift control, power electronics, pulsewidth modulation, safe operation area (SOA), short timescale, three-level converter.**

I. Introduction

In THE traditional research on power electronics, dynamic processes are often neglected, and only the steady states of "0" or "1" are of concern. Such research fails to grasp the failure mechanisms, dynamic processes, and unusual pulsed power phenomena of power electronic systems. Since most of the failures occur not in the steady states but in the fugacious commutating and switching process, the characteristics and causes of various abnormal pulses must be studied in detail in order to understand the failure mechanism. The approach that treats the waveforms as the synthesis of a fundamental wave and harmonics is somewhat helpless for fault analysis in real applications.

State-of-the-art power electronic research on short-timescale phenomena includes the semiconductor switching process, the commutating process, electromagnetic pulses, and carrier diffusion and drift in semiconductors. Reference [1] proposed that a typical power electronic system should include three interactive components, as shown in Fig. 1: 1) energy modulation; 2) energy loop; and 3) energy storage. More attention should be focused not only on the macroscopic energy modulation (the control algorithm), but also on the microscopic energy transfer and storage.

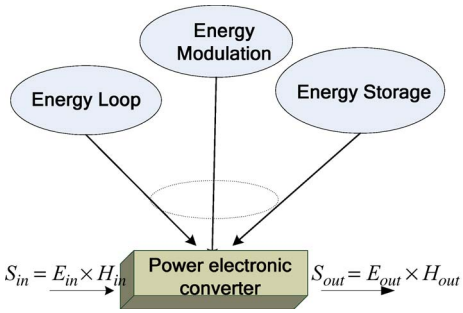

Fig. 1. Typical power electronic device [1].

The research on semiconductor devices has attracted substantial attention because of its significance in analytical modeling, fault precaution, and the appropriate applications of power semiconductor devices [2]–[5]. Reference [6] systematically studied the energy transfer process in the pulse transmission path, from semiconductor to turn-on and turn-off snubber and then to the dc rail. Reference [7] analyzed the traveling and standing waves on cables between motors and inverters and proposed different topologies to mitigate overvoltage in adjustable-speed drive (ASD) systems. Reference [8] studied the electrical pulses sharpened in the nonlinear transmission lines and lumped circuits and proposed that solitary waves exist in such networks. The method utilized in [9] is also popular in analyzing transmission-line modeling (TLM) problems, particularly in nonlinear components and nonlinear circuits.

However, all of the above approaches have some limitations, including the following.

1) *Lack of samples*. The samples of dynamic processes and summary of the characteristics are not adequate. Various short-timescale pulsed power phenomena would emerge, particularly in the conditions of high voltage, high power, and high power density, where the energy transformation and exchange are drastic.
2) *Lack of general research methodology*. Most of the present research is topology-specific. In fact, there are

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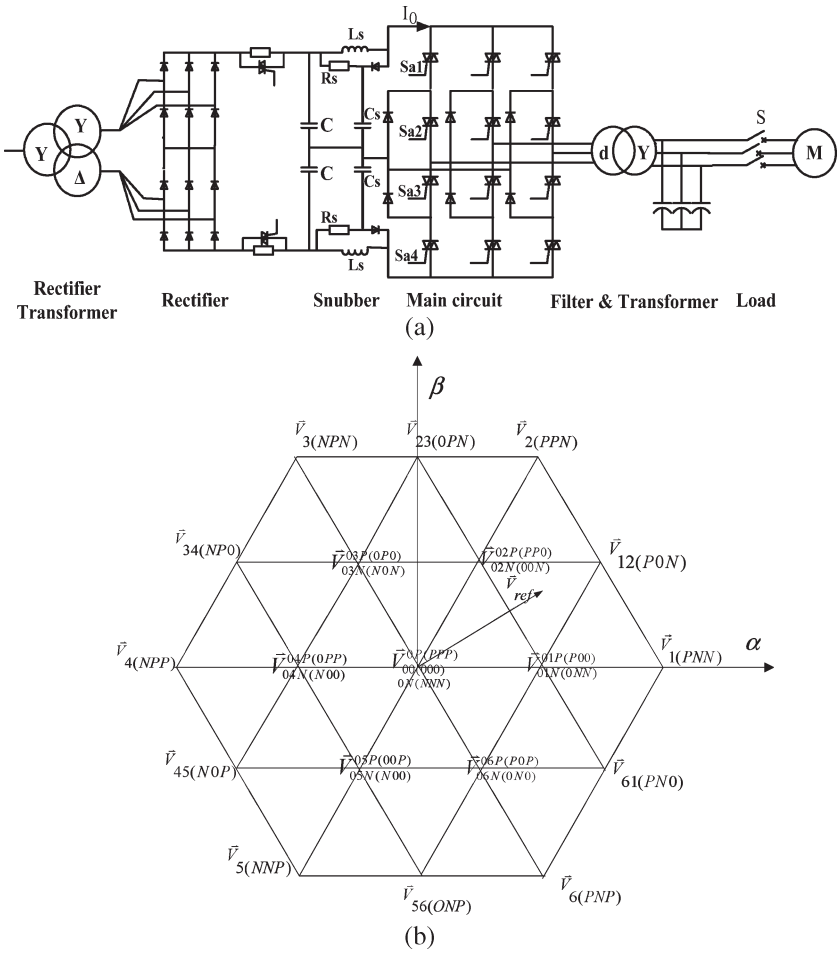

Fig. 2. High-voltage three-level inverter. (a) Main circuit topology of the three-level NPC inverter. (b) Vector distribution of the three-level SVPWM.

many common aspects in different types of power electronic converters, such as dc–dc converters and dc–ac inverters. The operation of all power electronic converters complies with the principle of energy conservation. Many of the concepts and principles for one type of converter shall be applicable to the others.

3) *Lack of integrated research*. The abnormal short-timescale pulsed power phenomena are the result of various factors. Most of them are caused by the interaction between the control algorithm, power devices, and peripheral circuits.

Based on two different prototypes, a three-level neutral point clamped (NPC) 6000 V/1.25 MW inverter and a 600 V/10 kW isolated bidirectional dc–dc converter, the safe operation area (SOA) of the systems are presented in Section II. In Section III, abnormal electrical pulses emerging in the real operations are classified according to their causes. Simulations and experiments are performed to validate the theoretical analyses. Based on these abnormal pulses, a new concept "*sneak pulse*" is introduced in Section IV. The design principle of power electronic devices is proposed to eliminate the sneak pulse by combining the macroscopic control algorithm with the microscopic transient process. In Section V, the concept of "*transient commutating topology*" is proposed, which is different from the traditional topology in commutating process research. In Section VI, accumulated errors in different prototypes are emphasized and solved by different strategies. In Section VII, the novel concept "*energy dead band*" is introduced for the isolated bidirectional dc–dc converter. Section VIII summarizes the contributions of this paper.

II. SOA of Power Electronic Systems

The overall topology and control algorithm of a three-level high-voltage inverter are shown in Fig. 2(a). The main circuit consists of a dc bus, snubber circuits, bridges, and the load. The switching devices are integrated gate commutated thyristors (IGCTs). In order to achieve voltage smoothing, boosting, and isolating simultaneously, a step-up transformer is utilized with its equivalent leakage inductance behaving as a filtering component. The smoothing capacitors are connected in parallel with the motor terminals. Fig. 2(b) shows the voltage vector distribution of the three-level space vector pulsewidth modulation (SVPWM).

Fig. 3 shows the circuit topology of the isolated bidirectional dc–dc converter, where the high-frequency transformer is used for isolation. Either H-bridge can be used as the primary while the other H-bridge as the secondary by phase-shift control.

In the operation of the power electronic converters shown in Figs. 2 and 3, some faults and abnormal pulses were observed.

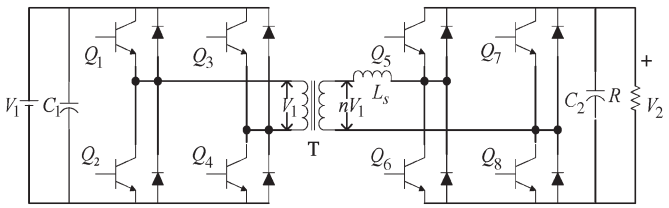

Fig. 3. Main circuit topology of the isolated bidirectional dc–dc converter.

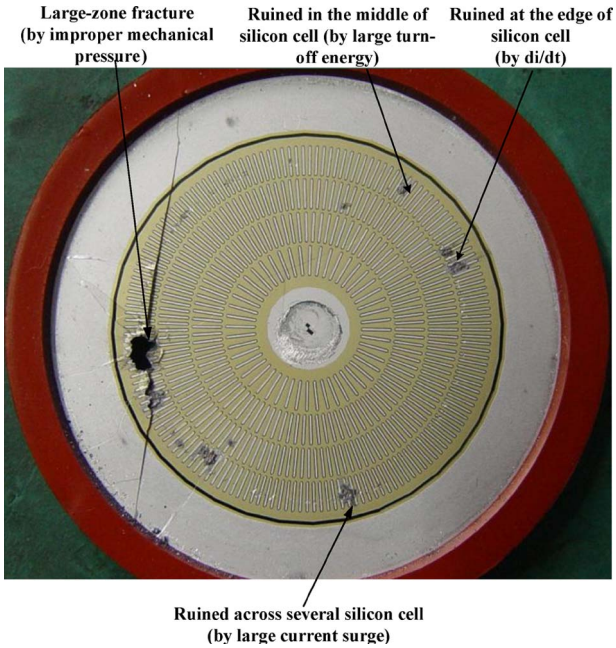

Fig. 4. Failure traces of IGCTs and fault analysis.

Although these failures appeared in different places and at different times with different causes, most of them are due to short-timescale phenomena.

A. Failure of Semiconductor Devices and SOAs

Failures of semiconductors encountered frequently as shown in Fig. 4 are observed in the high-power three-level prototype. They can be high current, high-voltage, high di/dt, high local convergence of turn-off energy, etc. When analyzing the cause of such failures, it is worth noting that the operation of a semiconductor device will be influenced by other semiconductor switches as well as passive components in the circuit, parasitic parameters, operation modes, and load conditions. The traditional SOA for a single semiconductor provided by the datasheet based on buck test circuits is not possible to always include all the above factors. Therefore, it cannot guarantee the reliability of the overall system, which may employ a different topology than the test circuits. Hence, the device-level SOA should be reconsidered.

The datasheet-based device-level SOA is helpful but does not demonstrate the system ratings. A new concept, called "system-level SOA" (SSOA), is proposed in this paper. SSOA is not only determined by the operation conditions, such as voltage and current, but also by many other circuit parameters. For example, for the high-voltage three-level NPC inverter studied in this paper, an excessive dc voltage can damage the IGCT. However, a lower dc voltage would result in high output current in order to maintain the rated output power. Thus, a high-voltage spike on the IGCT during the turn-off process will be induced by the parasitic inductance, which can also damage the semiconductor device. The SSOA must ensure the overall system safety, as shown in Fig. 5(a), where the horizontal axis is one-half the dc-link voltage, not the single-device voltage defined by the traditional device-level SOA in the datasheet. Based on the SSOA, after considering the influence of stray inductance, di/dt, voltage endurance, system rated power, voltage modulation index by SVPWM, and transformer turns ratio (2200 V/6000 V), the feasible range for the devices is reduced to [1400 V, 2700 V].

The vertical axis of Fig. 5(a) represents the maximum repetitive turn-off current. The lighter shadow area is for a single IGCT defined by the datasheet [10], and the denser shadow area is for the SSOA. The design of the system should not exceed the region defined by the SSOA [11].

In the bidirectional 10 kW/600 V dc–dc converter, the voltage endurance could be handled easily. However, since both the supply and the load can be voltage sources, the current impact must be considered. The maximum current will be constrained by the leakage inductance $L_{\rm s}$ of the isolation transformer. However, a larger $L_{\rm s}$ will decrease the power capability of the converter. Hence, the key step for an SSOA design of bidirectional dc–dc converters lies on the selection of $L_{\rm s}$ to depress the current impact and increase the output power, as shown in Fig. 5(b). For example, if the switching frequency is chosen as 10 kHz, the leakage inductance should be designed to be within the interval defined by A3.

B. Distortion of Drive Signals

The pulse distortion is observed, as shown in Fig. 6(a), during the operation of the power electronic converters. This distortion is caused by the circuit parasitic parameters. The parasitic inductance of the wires between the IGBT gate and the drive signal generator distorts the drive signals and possibly causes the failure of the intended switching actions. In Fig. 6(b), one of the interlocked switches does not fully turn on. In order to minimize the effect of parasitic parameters and prevent the fault conditions, coupled and twisted wires with minimum stray inductance can be used [1].

III. Output Voltage Distortion of Power Electronic Systems

Investigation of the mechanisms of different waveforms is important as the first step to recognize the pulsed power phenomena in power electronic systems. In the operation of power electronic systems, numerous abnormal PWM pulses may exist. The mechanisms and profiles of these abnormal pulses are multiform. Dead band, minimum pulsewidth, snubber circuit, parasitic parameters, switching performance of semiconductor devices, and load characteristics are all possible causes of these short-timescale phenomena.

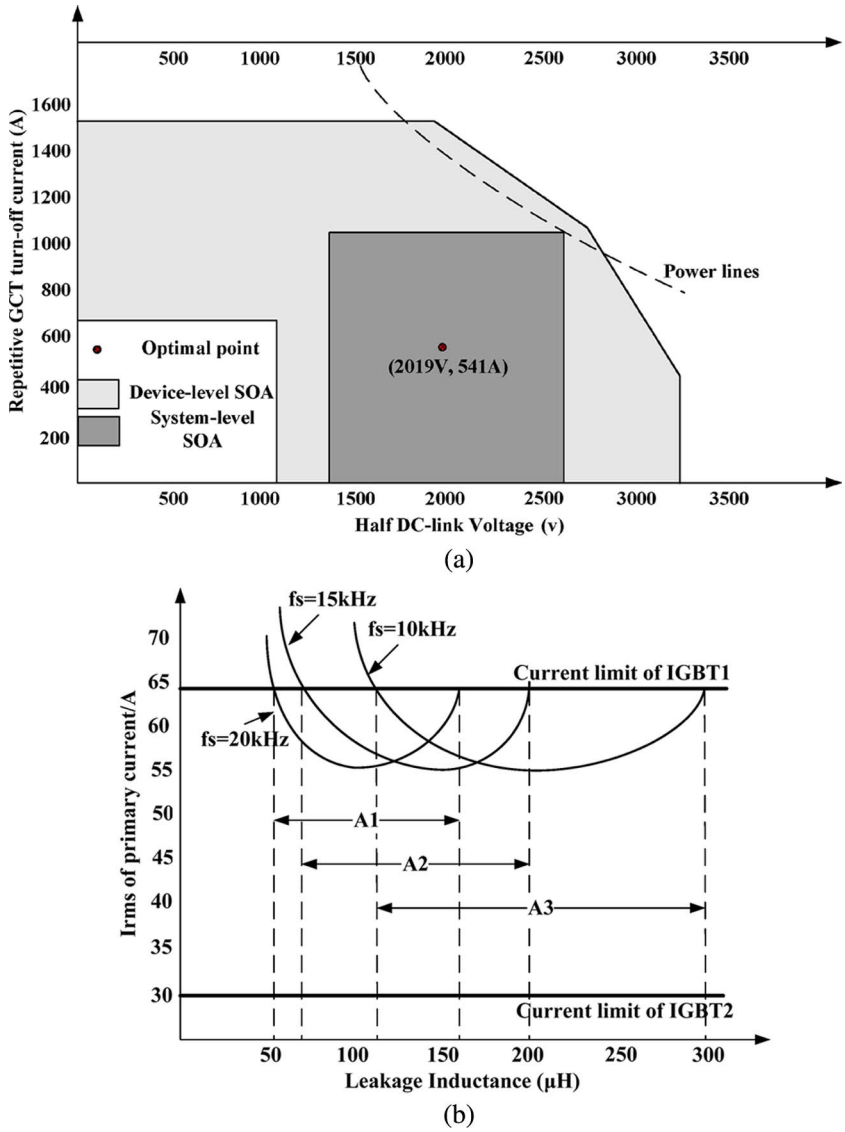

Fig. 5. SSOA design for power electronic converters. (a) SSOA for a three-level inverter. (b) SSOA for a dc–dc converter.

A. Abnormal Pulse Caused by the Control Algorithm

In order to avoid a breakthrough of the bridge in the commutating process, a dead band is imposed on the gate drive signals of the two interlocked semiconductor devices. During the dead band, the output voltage is in an uncontrolled state. Voltage distortion will occur due to the dead-band effect [12]. Traditional research assumes that the output current of an inverter remains in one direction during one switching period. Assume the output current is positive when it flows from the inverter to the motor, phase B current (I_{B}) is positive, and phase C current (I_{C}) is negative, as shown in Fig. 2(a). The line–line voltage V_{CB} in one switching period T_{s} would behave as shown in Fig. 7(a) without a dead band and in Fig. 7(b) with a dead band. These are symmetric pulses.

However, measurements of the three-level 6000 V/1.25 MW ASD system indicate an asymmetrical pulse sequence in one period T_{s}, as shown in Fig. 7(c). The simulation shown in Fig. 7(d) confirms that I_{B} is oscillating near zero while I_{C} remains negative. The dead-band effect does not show in phase B.

The asymmetric pulses distorted by the dead band are mainly due to the control algorithm, where the dead band is inserted with load current oscillating near zero.

The above analysis is based on the condition where current changes direction in one switching period. Under some circumstances, the current can change direction a few times in one dead band, as observed in the isolated dc–dc converter. In traditional low power dc–dc converters with high switching frequency (for MOSFET) [13], [14], a large dead band is not necessary. However, in high-voltage and high-power application, a dead band is essential in guaranteeing the safe operation of the system.

Fig. 8 shows a comparison between the line–line voltage of a dc–ac inverter and that of a dc–dc converter. *Pulse 1* in Fig. 8(a) is caused by the current zero-crossing in one dead band and only occurs at specific load conditions, which are often ignored. Fig. 8(b) shows the measured primary voltage (channel 1), secondary voltage (channel 2), and primary current (channel 3) in the dc–dc converter. The cause of distortion in

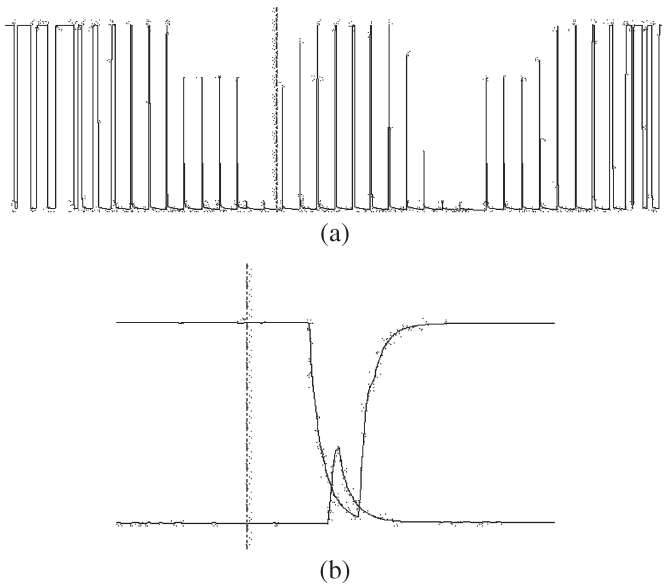

Fig. 6. Distorted gate signals. (a) Drive-signal sequence on one IGBT gate. (b) Gate signal of the two interlocking IGBTs.

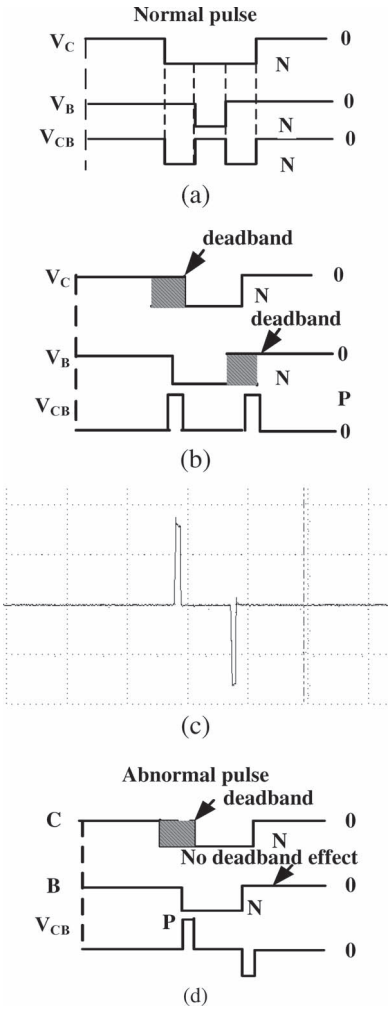

Fig. 7. Dead-band effect in a three-level high power inverter. (a) Without a dead band (symmetric pulses). (b) With a dead band (symmetric pulses). (c) With a dead band (asymmetric, experiment). (d) With a dead band (asymmetric, simulation).

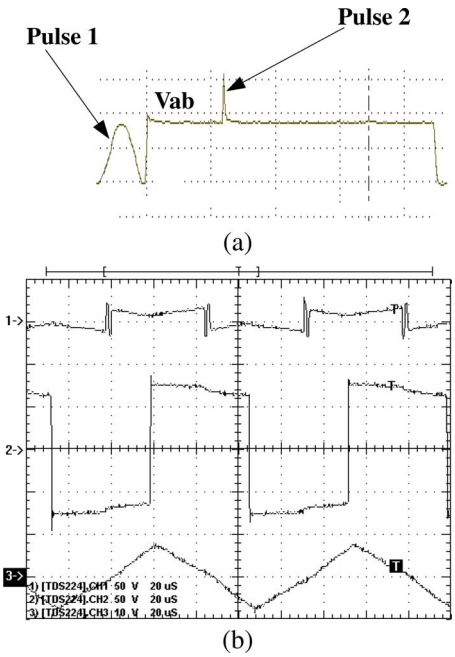

Fig. 8. Control abnormal pulse. (a) Distorted waveform of $V_{\rm ab}$ in a three-level inverter. (b) Voltage distortion in a dc–dc converter.

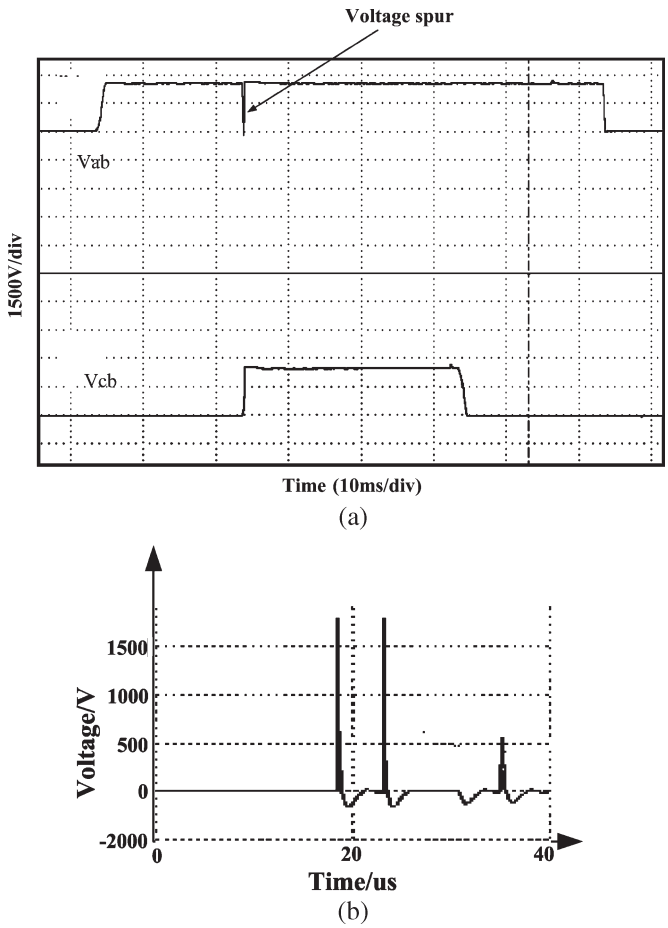

Fig. 9. Experimental and simulation waveforms for a circuit abnormal pulse. (a) Experimental waveforms of $V_{\rm ab}$ and $V_{\rm cb}$. (b) Voltage spurs on a snubber inductor.

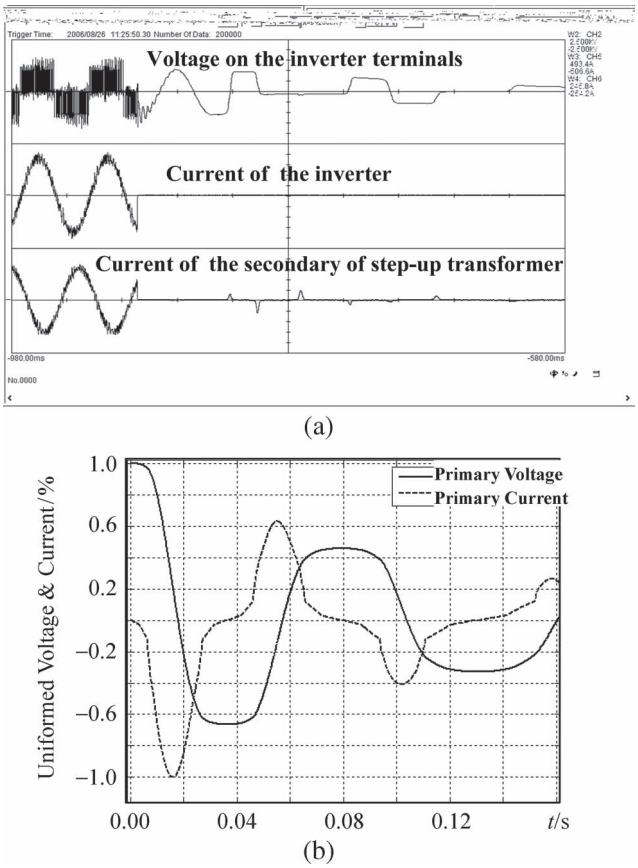

Fig. 10. Voltage/current waveforms on the terminals of 6000 V/1250 kW inverters under fault protection where all the IGCTs are turned off simultaneously. (a) Experimental line–line voltage/current waveforms of the inverter in the process of fault protection. (b) Simulated line–line voltage/current waveforms of the inverter in the process of fault protection.

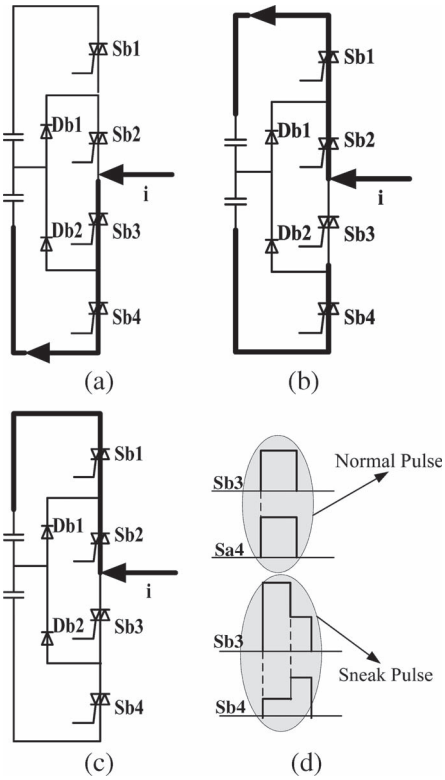

Fig. 11. Sneak pulse in dc pre-excitation. (a) Level N. (b) Sneak pulse on Sb3. (c) Level P. (d) Sneak pulse.

the primary voltage is the same as in Fig. 8(a). Such abnormal pulses are encountered primarily in the isolated bidirectional dc–dc converter where the current changes direction in the dead band.

B. Abnormal Pulse Caused by Circuit Parasitic Parameters

The abnormal voltage spurs such as pulse 2 in Fig. 8(a) and that in Fig. 9(a) sustain for 4 μs. Frequently, these spurs appear at the moment when one bridge begins commutating while the other two bridges remain in steady state. Simulation reveals that these spurs are in coincidence with the voltages on the snubber inductor, as shown in Fig. 9(b).

The main reason for these special spurs lies on the fact that only one set of snubber circuit is applied for the three-bridge inverter shown in Fig. 2(a). The commutating process in one bridge would alter the current flowing through the snubber inductor, which induces voltage drop on the snubber inductor. Therefore, the output voltage levels of the other two bridges will be affected. Since this effect is due to the existence of the snubber circuit, these abnormal pulses are caused by *circuit parameters*.

C. Abnormal Pulses Caused by Control and Circuit

Ultimately, most of the abnormal pulses are the result of the combination of control and circuit. For example, in Fig. 2(a), during fault protection, the inverter should be isolated from the load, and the circuit breaker S will be off. All the IGCTs are turned off as shown in Fig. 10. The inverter behaves as a rectifier. The energy of the smoothing capacitors will be transferred to the step-up transformer and the inverter. The abnormal pulses are observed on the primary terminals of the transformer.

1) The primary line–line voltage behaves as square waveforms.
2) The primary current of the step-up transformer takes the shape of a pulsating waveform.

Simulation shows that these pulsed waveforms attribute to the switching off of S, pulse blocking of the inverter, and nonlinear characteristics of the step-up transformer [15]. Nonzero current implies that the energy flows from the capacitors and transformer back to the inverter. When the current exceeds a certain threshold, the inductance of the transformer decreases significantly due to saturation of the core and induces the aberrations of voltage and current.

IV. Sneak Pulse

The former three types of abnormal pulses may not affect the reliability of the inverters. In some less-likely circumstances, there are unexpected pulses that could damage the whole system. These could be defined as a "*sneak pulse*."

One example is the sneak pulse in the dc pre-excitation of the three-level inverter [16]. Vector **PPP** and **PNP** shown in Fig. 2(b) are utilized to establish the dc magnetic field before starting up in order to depress the current impact on the motor.

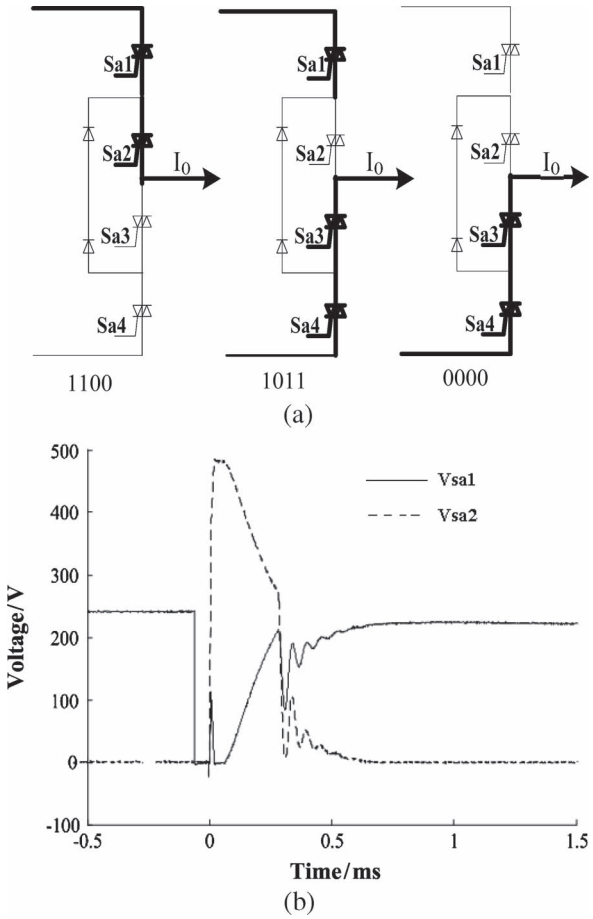

Fig. 12. Sneak pulse in the pulse-blocking process. (a) Sneak pulse in the commutating process. (b) Measured sneak pulse.

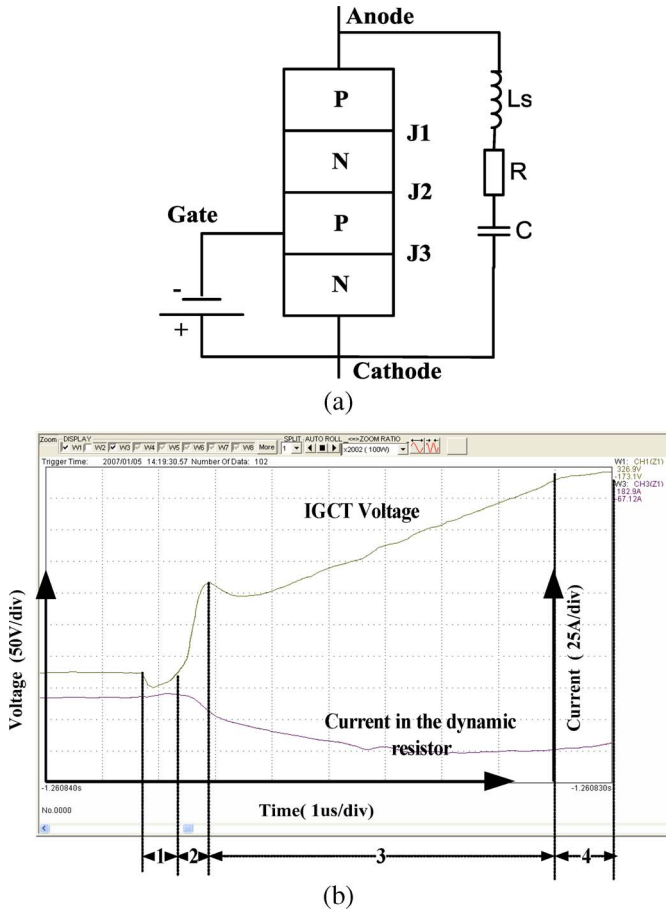

Fig. 13. Waveforms of series-connected IGCTs. (a) IGCT structure and RC snubber. (b) Turn-off voltage and current waveforms.

For **P**, the voltage output is Vdc/2, and the four switches are set to [1100]; for **0,** the voltage output is zero, and the four switches are set to [0110]; and for **N**, the voltage output is $-$Vdc/2, and the four switches are set to [0011], where 0 means the OFF state and 1 means the ON state of the switches.

When the output voltage switches from **N** to **P** for phase B, although Sb3 and Sb4 are triggered simultaneously, Sb3 might be off prior to Sb4 due to the difference in the real time sequence or the inherent characteristics of different semiconductor devices. This will cause one device to overtake the whole dc voltage and destroy the whole bridge, particularly in the high-voltage inverter, as shown in Fig. 11.

The voltage pulse on Sb3 in Fig. 11(b) is the sneak pulse, whose waveforms are illustrated in Fig. 11(d), where the voltage sharing is not uniform. To eliminate such a sneak pulse, a modified algorithm is required. For example, the optimal vectors **0NP** and **000**, instead of **PNP** and **PPP**, have been proven to be effective to eliminate the above sneak pulse [16].

Such phenomena also occur in the motor braking process. In this process, hypothetically, all the semiconductor devices in the bridges are turned off simultaneously. However, the difference in the real time sequence of the gate signals can result in one semiconductor undertaking the whole dc bus voltage, as shown in Fig. 12, where Sa2 is turned off prior to Sa1, Sa3, and Sa4. When Sa2 is turned off, with $I_0 > 0$, the current is quickly commutated from Sa1 and Sa2 to the parasitic diodes of Sa3 and Sa4. At that time, Sa1 is still on, which makes Sa2 undertake the whole dc-link voltage. This is very similar to Fig. 11. Algorithm optimization, which is similar to the selection of voltage vectors in the pre-excitation process, should be revised [17].

These sneak pulses have close relations with the control algorithms and circuit topology. For example, if each semiconductor device is equipped with a turn-off snubber circuit, such as an RC snubber, the sneak pulse will not be predominant. In two-level dc–dc converters, such a sneak pulse will not occur either.

V. Transient Commutating Topology

Research of the above abnormal pulses, including the sneak pulses and SSOA, is beyond the conventional topology because the pulses occur in the commutating process with high interaction between the control algorithm, circuit parameters and semiconductor characteristics. A novel concept, namely, the "transient commutating topology," is proposed in this paper. It is a topology combining the parasitic parameters in the loop, switching characteristics of semiconductors, control algorithms, and the load characteristics. Furthermore, it is a dynamic and time-varying topology. In a more general term, it is a combination of energy modulation, energy loop, and energy storage.

Transient commutating is defined as the commutating process where an electromagnetic pulse is generated by energy

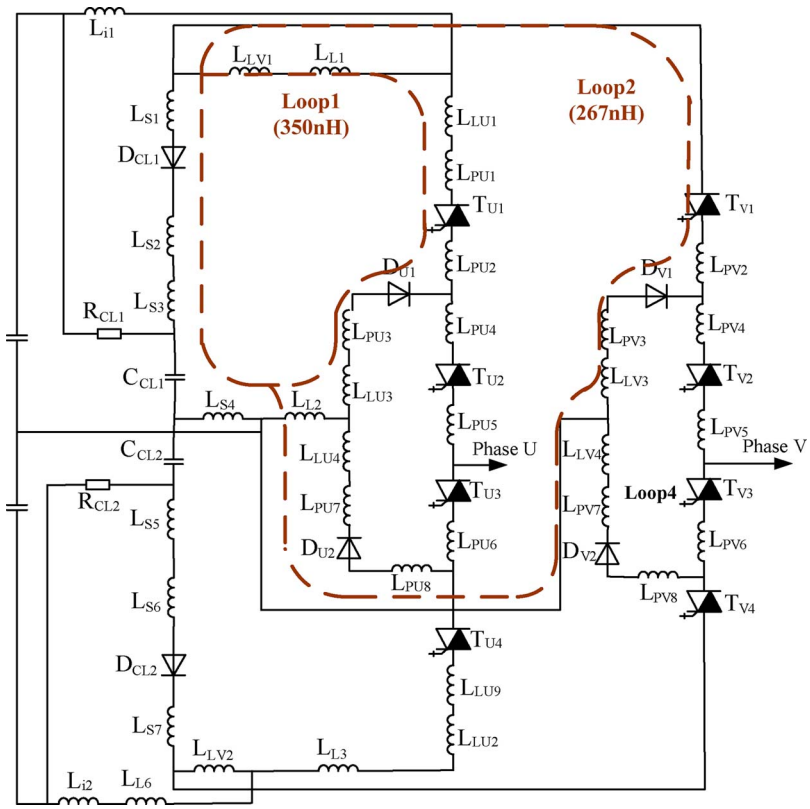

Fig. 14. Transient commutating topology.

modulation strategy and modified by the energy storage components and parasitic parameters of the energy transmission loop. Although this concept contains the traditional topology, it is mainly attributed to the commutating process.

In the transient commutating topology, the stray parameters, the control algorithms, the semiconductor performance, and the load characteristics should be considered. It should be noted that this topology is similar to a comprehensive analysis method other than the ideal topology.

A. Topology of IGCT During Turn-Off

When the semiconductors, such as IGCTs, are in series connection, the high-voltage RC snubber circuit is used to balance the voltage sharing between different IGCT modules, as shown in Fig. 13(a) [18]. When the IGCT is turned off, the voltage and current waveforms are illustrated in Fig. 13(b) [19].

There are four main stages in the above waveform.

Step 1) A negative voltage is applied to the IGCT. The voltage has an amplitude of 20 V and is equal to the gate drive voltage. Fig. 13(a) shows the IGCT structure in the turn-off process, where -20 V is imposed on junction J3 to commutate the current from GCT to Gate. Since junctions J1 and J2 are not off yet and do not withstand any voltage, the voltage across anode and cathode is the voltage across J3, e.g., -20 V, which makes current flow reversely in the RC circuit.

Step 2) Both current i and di/dt increase, which induces the first voltage spike. Simulation shows that the first voltage spike is caused by the stray inductance L_s, which will limit the turn-on di/dt but induce the voltage spike in the turn-off process. Therefore, a low-inductance resistor and a capacitor are necessary.

Step 3) Current i increases, and di/dt decreases. The voltage across the IGCT is mainly the voltage drop on resistor R and capacitor C.

Step 4) Current i decreases, and the capacitor is continuously charged.

In this example, to simplify the details of the electrical waveforms, the structure of the IGCT, gate signal generation, and parasitic parameters in the peripheral circuit are all involved. In order to simulate this process, a functional model of semiconductor needs to be built [20], [21].

B. Topology of a Three-Level Inverter

For the two bridges of three-level converters, the traditional topology assumes that the semiconductors, such as IGCTU1 and IGCTV1 in Fig. 14, undertake the same voltage stress during the switch-off process. However, in Fig. 14, a tremendous amount of stray inductance contributes to the commutating process. They exist in the loop consisting of snubber diodes (e.g., $\mathrm{Ls}_1-\mathrm{Ls}_6$), clamped diodes, IGCTs, etc.

Due to different commutating loops and different distances from the snubber circuit, the parasitic inductances of the

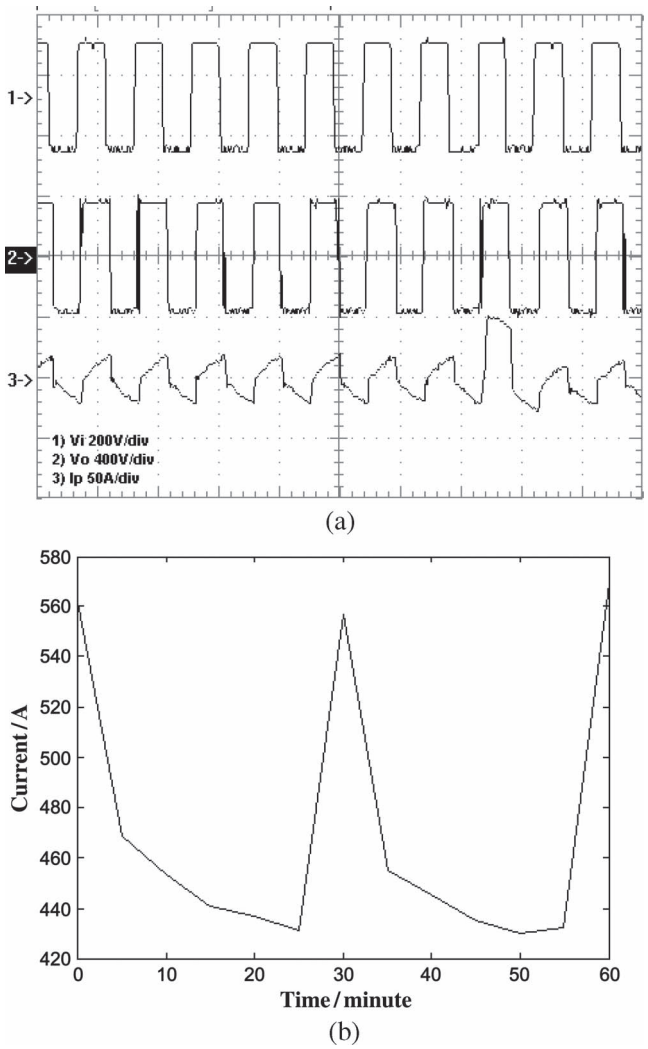

Fig. 15. Accumulated errors in the different power electronic systems. (a) Current oscillation in a dc–dc converter. (b) Current oscillation in a three-level inverter.

commutating loop for different IGCTs vary. For example, when the state of bridge U changes from [1100] to [0100] and current is outside the bridge, IGCTU1 turns off. The commutating loop is Loop1 in Fig. 14, where the total inductance is $L_1 = 350$ nH. Similarly, when IGCTV1 turns off, the commutating loop is Loop2 with stray inductance $L_2 = 267$ nH. The reason that $L_2 < L_1$ lies in the real application where the snubber circuit is equipped close to bridge V while a little farther away from bridge U. Note that Fig. 14 is only a flat schematic, not the real 3-D one. The unequal distance from the snubber circuit makes the inductive voltage spikes undertaken by different IGCTs. More detailed calculations can be found in [22].

Based on the transient commutating topology, in order to achieve high-performance energy transformation and transmission, not only the control algorithm, but also the energy loop and the energy storage, should be optimized to eliminate the abnormal pulses or the sneak pulses. It is a combination of microscopic electromagnetic transients and the macroscopic control algorithm. In Fig. 14, stray parameters of different phases should be minimized, and the difference of distance of the bridges from the snubber circuit should be considered.

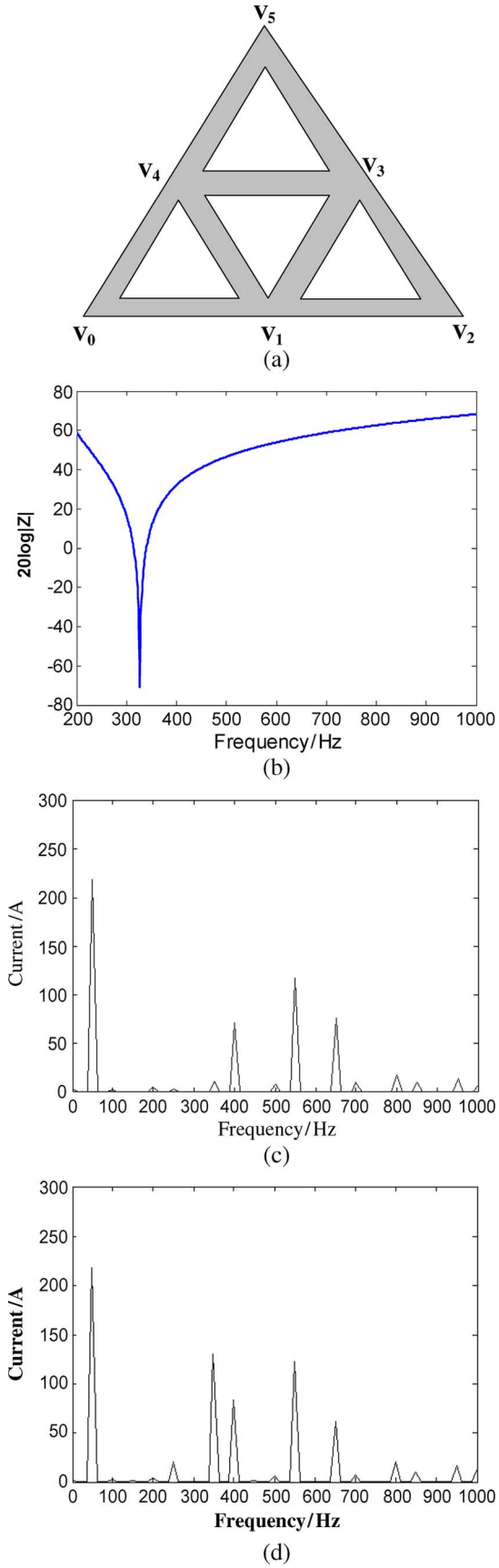

Fig. 16. Influence of the minimum pulsewidth and the LC characteristics. (a) Restricted area by the minimum pulsewidth. (b) Impedance characteristics of an LC filter. (c) Current spectrum without the minimum pulsewidth. (d) Current spectrum with the minimum pulsewidth.

In Fig. 8(a), in order to eliminate pulse 2, each bridge should have a snubber circuit. However, this will increase the overall system cost.

VI. Accumulated Error

The accumulated error in the control algorithms deviates the real pulses from the intended ones imposed on the load. The causes and behaviors are different in different systems. For example, in the isolated bidirectional dc–dc converter, the phase shift between the gate signals of Q_1 and Q_5 in Fig. 3 is generated by a microprocessor, a DSP, or microcontrol chip UC3875. With the analog design, it was observed that a small disturbance on this phase shift is a predominant factor disturbing the safe operation, particularly at the boundary conditions where $V_2 = nV_1$. Simulation proves that this is the most unstable operation point in the dc–dc converter. An accumulated error in the phase shift could result in current oscillation and even trigger the current protection. Such an error is mainly caused by the proportional–integral modulators and causes the variation of the current peak. It could be depressed by increasing the leakage inductance to realize a more robust system. Fig. 15(a) shows the current oscillation caused by the experimental accumulated error in the dc–dc converter.

An accumulated error is also prevalent in the high-power three-level inverter. Fig. 15(b) shows the statistics of the measured output current of the inverter over time. Every 30 min, the current amplitude will oscillate once. Simulation shows that the accumulated error in the calculation of the voltage vector angle would make the real voltage vector gradually deviate from the calculated one. If the vector angle shifts into the region restricted by the minimum pulsewidth illustrated in the shadow area of Fig. 16(a), the harmonics in the output voltage will increase. Some of these harmonics will be amplified by the LC impedance characteristics shown in Fig. 16(b) and result in a low-frequency oscillation of the current amplitude, as shown in Fig. 16(c) and (d).

A comparison of Fig. 15(a) and (b) shows the common aspect of accumulated errors in the dc–dc converter and the three-level inverter. These errors are all generated by the control algorithm, amplified by the peripheral circuit (for the dc–dc converter, it is the leakage inductance; for the inverter, it is the LC filter) and occur in the short-timescale process.

VII. Energy Dead Band

The purpose of a dead band is to avoid a bridge breakthrough. For a two-level dc–ac inverter, energy could only flow from the load to the bridge in the dead band. In a dc–dc converter, the supply and load could be exchanged. In some circumstances, they both behave as load and the isolated transformer becomes the supply. This is the *energy dead band*.

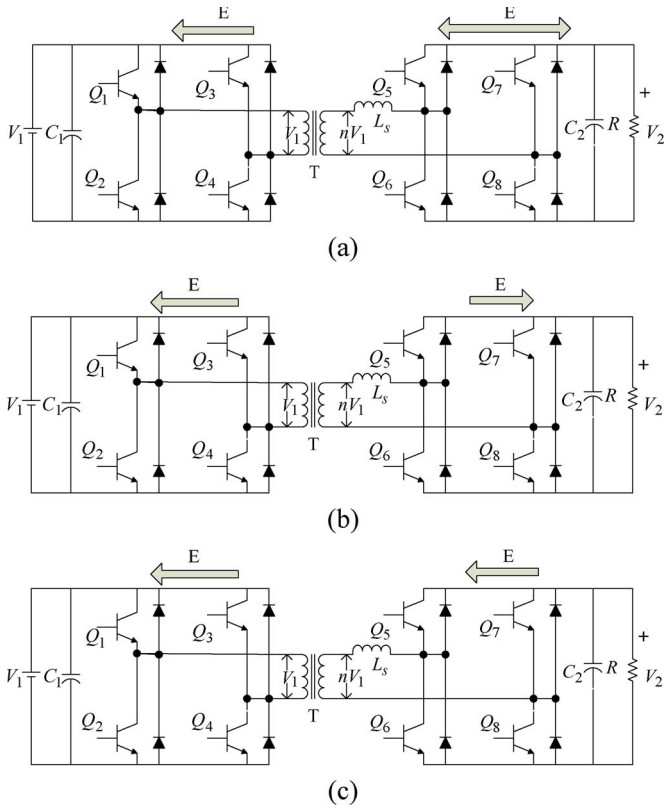

Fig. 17. Energy flow in the extreme time sequence during (a) interval Δ_1, (b) interval db_2, and (c) interval Δ_2.

The time sequence of the gate signals of Fig. 3 is

$$Q_2/Q_3 \quad \text{OFF} \quad \underset{\rightarrow}{db_1} \quad Q_1/Q_4 \quad \text{ON} \quad \underset{\rightarrow}{\Delta} \quad Q_6/Q_7 \quad \text{OFF} \quad \underset{\rightarrow}{db_2} \quad Q_5/Q_8 \quad \text{ON}$$

where db_1 and db_2 are the dead bands of the primary bridge and secondary bridge, respectively. If the primary side current is different from that of the secondary, the dead bands of the two bridges are usually not equal. Suppose $db_1 > db_2$. If the load is light, there will exist one extreme condition where the time sequence of the gate signals on the semiconductors is described by the expression shown at the bottom of the page, where $db_1 = \Delta_1 + db_2 + \Delta_2$. The energy flow diagram during the interval is illustrated in Fig. 17.

It can be seen in Fig. 17 that there is always an overlapped region where energy does not flow from one side to the other, but from the transformer to the two dc sides. At this moment, the energy stored in the leakage inductance will be consumed up very quickly. Afterward, the current will remain zero and will cause the oscillation of the voltage drop on the leakage inductance, as shown in Fig. 18, where G_1 stands for the gate signals of Q_1 and Q_4, G_2 for Q_2 and Q_3, G_3 for Q_5

$$\overrightarrow{db1}$$

$$Q_2/Q_3 \quad \text{OFF} \quad \underset{\rightarrow}{\Delta_1} \quad Q_6/Q_7 \quad \text{OFF} \quad \underset{\rightarrow}{db_2} \quad Q_5/Q_8 \quad \text{ON} \quad \underset{\rightarrow}{\Delta_2} \quad Q_1/Q_4 \quad \text{ON}$$

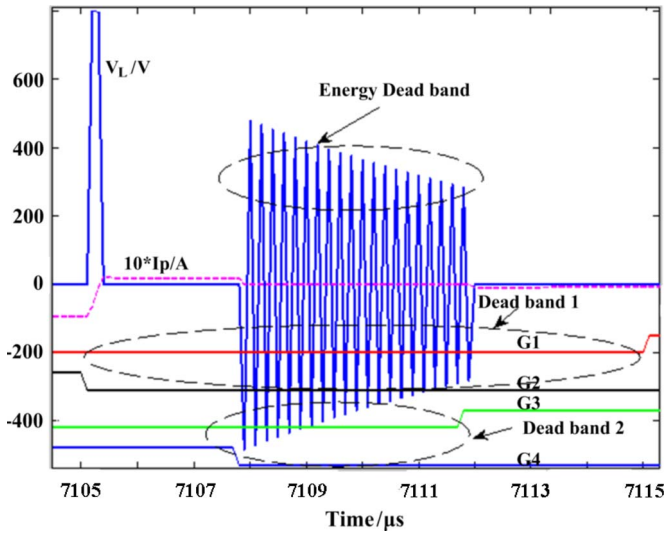

Fig. 18. Energy dead band in the dc–dc converter.

and Q_8, and G_4 for Q_6 and Q_7. Such a switch mode is very similar to the discontinuous mode in conventional buck or boost converters.

Energy dead band is a special phenomenon in isolated bidirectional dc–dc converters. The precondition of energy dead band is light load and small shift angle, as well as different dead band settings in the primary and secondary bridges. In the energy dead band, the transformer, or, more generally, the energy storage component, acts as the power supply, and the original power supplies serve as load. Energy in the leakage inductance will be distributed evenly to the two dc buses. The whole system, from power supply to load, is in an uncontrolled state.

VIII. Conclusion

Research on short-timescale pulsed power phenomena in high-voltage and high-power electronic system is crucial for realizing reliable power electronic systems and achieving high-performance power conversion. The main methodology of this research is to probe these transient processes in short timescales. In this paper, by studying the samples from different power electronic systems, related influential factors and mechanisms of these abnormal pulsed power phenomena have been investigated in detail. Four new concepts are proposed in this paper: 1) SSOA; 2) sneak pulse; 3) transient commutating topology; and 4) energy dead band. These concepts are well supported by experiments of the two prototypes.

The design of power electronic systems is increasingly more toward combining the macroscopic algorithms and microscopic pulses, assuring the SSOA for the system, and reducing the probability of sneak pulse through optimization of the energy modulation, energy transmission loop, and energy storage components.

The transient commutating topology is proposed to illustrate the dynamic and time-variant commutating process with the consideration of energy loop and control strategy. It is related to the energy transmission. Accumulated errors are validated by different prototypes. Their causes are different, so the solutions are also different. In the three-level inverter system, it is caused by the minimum pulsewidth. In the isolated dc–dc converter, it is caused by the modulator.

An energy dead band is found in the isolated bidirectional dc–dc converter where no energy flows in the common energy transmission loop. It is believed that in multilevel inverters, there should be a similar phenomenon that needs to be explored. Further experiments on other power electronic systems are necessary to explore other aspects of these new concepts to form a more comprehensive theory framework on the short-timescale pulsed power phenomena.

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