The Short-Time-Scale Transient Processes in High-Voltage and High-Power Isolated Bidirectional DC–DC Converters

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***Abstract*—This paper discusses the short-time-scale transient processes in an isolated bidirectional dc–dc converter with phase-shift control. The deadband effect on the steady-state and transient commutating process are analyzed. The current variations caused by phase-shift errors at the boundary conditions are simulated and validated through experiments. The concept of "energy deadband" is introduced to describe those specific transients where no energy flows from source to load or load to source. A set of strategies are proposed to increase the system robustness. Simulation and experiments on a 200-V/400-V, 6-kW dc–dc converter prototype validated these strategies.**

***Index Terms*—DC–DC converter, deadband effect, high-frequency transformer, phase shift, short-time-scale, transient process.**

I. Introduction

THE dc–dc converter is a key component in hybrid electric vehicles (HEVs) to manage power flow and maintain battery health. Electrical isolation may be required to provide safe operation for the equipment operated on the hybrid battery, such as in military applications. State-of-the-art isolated dc–dc converters are generally based on single-phase full-bridge topologies with isolation transformers [1], [2].

Fig. 1 shows a typical scheme of an isolated bidirectional dc–dc converter, which consists of dual H-bridges located on the primary and secondary sides of an isolated transformer, respectively. The primary bridge consists of four switches, Q_1, Q_2, Q_3, and Q_4, which are commonly insulated gate bipolar transistors (IGBTs) for high-power applications. The second H-bridge also consists of four switches, Q_5, Q_6, Q_7, and Q_8, which are connected to the secondary winding of the transformer. With a phase-shift control algorithm, the first H-bridge provides a square wave with duty ratio of 50% to the primary winding of the high-frequency transformer. The voltage of the secondary winding has a finite phase-shift angle from the primary voltage so as to transfer energy from the source to load or vice versa [3], [4]. In this process, the transformer's leakage inductance serves as an instantaneous energy storage component.

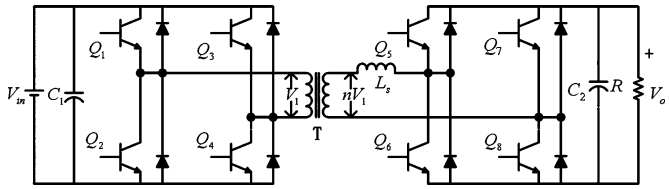

Fig. 1. Isolated bidirectional dc–dc converter system in an HEV.

The previous works on the full-bridge dc–dc converter mainly focused on the topology [5], [6], control strategies [7], [8], and macroscopic modeling methods [9]–[12] based on classical control theory. The microscopic short-time-scale transient processes, such as deadband effect and phase-shift error, have not been studied in detail. These phenomena are very important in real-world applications of modern power electronics [13], and have been discussed largely in dc–ac inverters [14], [15]. Although various deadband compensation techniques were proposed for inverter applications [16], [17], no similar research has been reported for isolated bidirectional dc–dc converters. Phase-shift error, or more generally, the error of pulse time sequence, is another important issue in the closed-loop system control, i.e., the real pulse applied to the devices may have a large deviation from the intended one, and therefore, cause the current to oscillate [18].

In traditional unidirectional dc–dc converters, the power ratings are generally low, and the switching frequency is relatively high (for MOSFET or SiC, turning on and off processes are both in the nanosecond level) [19]–[23]. Therefore, there is, generally, no need to deal with deadband effect. However, in high-voltage and high-power isolated bidirectional dc–dc converters, the deadband and phase-shift error will greatly affect the operation of the converter, both in steady-state and transient processes. These issues generally deteriorate the operational performance, or even damage the system under some specific switching conditions because of large unexpected current and voltage spikes.

This paper discusses the effect of deadband and the influence of phase-shift error. It also discusses the energy flow during the deadband and introduces a definition of "*energy deadband*." A set of strategies was simulated and relevant experiments on a 200-V/400-V, 6-kW prototype supported the study.

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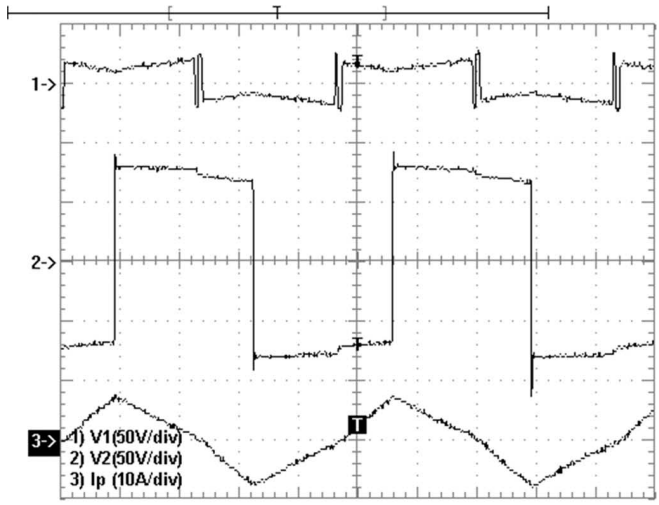
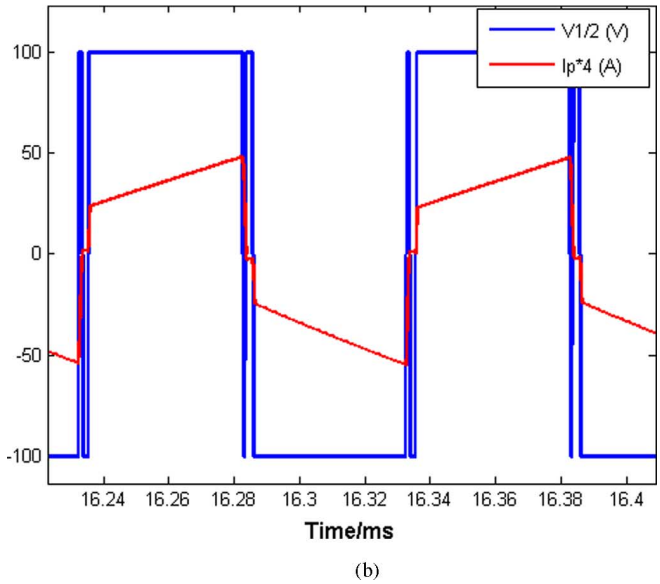


(a)



(b)

Fig. 2. Deadband effect on the primary voltage waveforms. (a) Experiment results. (b) Simulated results.

II. Short-Time-Scale Transient Processes

A. Voltage Variation During the Commutation Process

In full-bridge converters, in order to avoid shoot through of the bridge during commutation process, a deadband is inserted between the interlocked switches in the same bridge. Deadband is very crucial to guarantee the reliability of high-voltage and high-power converters.

In this study, the prototype converter is rated at 200 V/400 V, 6 kW with switching frequency of 10 kHz. The IGBTs of the primary H-bridge are rated at 65 A and the inherent deadband is 4.5 μs. The secondary bridge is rated at 30 A and the inherent deadband is 2.2 μs.

Although the deadband guarantees the safe operation of the system, it will cause waveform distortion and other unexpected short-time-scale transient processes, as shown in Fig. 2.

In the deadband, the polarity of output voltage depends on the current direction, which is called the deadband effect. During the deadband, all of the four semiconductors in the primary H-bridge, Q_1–Q_4, will be turned off. The common assumption is that the current direction remains the same in the deadband. However, if the inductor current changes direction during this interval, the output voltage of the bridge will change polarity. Therefore, the variations in the primary voltage shown in Fig. 2(a) will appear. Simulation shown in Fig. 2(b) validates this analysis. The variations in the primary voltage are caused by the change of current direction during the deadband. Similar phenomenon also existed in a three-level dc–ac inverter when the current has a large variation [18], which makes the traditional deadband compensation difficult to implement. In real-world applications, this variation will not deteriorate the system operation, but frequent variation of voltage waveforms may bring electromagnetic interference (EMI) and other issues.

B. Phase-Shift Error at the Boundary Conditions

The phase-shift between the gate signals of Q_1 and Q_5 are generated by a microprocessor, a DSP, or a microchip such as UC3875. In practice, it is found that a small disturbance on the phase-shift angle will cause the inductor current to oscillate near the boundary conditions, as shown in Fig. 3(a). This abrupt variation will ultimately affect the safe operation of the power switches. In the following analysis, the turns ratio of the transformer is $1{:}n$, the transformer primary voltage is V_1, DT_s is the phase shift between the two bridges, D is the duty cycle in one-half period T_s, I_{Ls} is the current of the equivalent leakage inductor of the secondary winding, and V_2 is the output voltage. The experimental waveforms of the current variations are shown in Fig. 4, where channel 1 is V_1, channel 2 is V_2, and channel 3 is the primary current.

Theoretical analysis shows that the output power is [7]

$$P = nV_1\bar{I} = \frac{nV_1V_2}{2f_sL_S}D(1-D). \tag{1}$$

The initial and maximum inductor current for $V_2 > nV_1$ is

$$\begin{cases} i(t_0) = \dfrac{1}{2\omega L_S}[(\pi-2\phi)V_2 - nV_1\pi] \\ \qquad = \dfrac{1}{4fsL_S}[-nV_1 - 2DV_2 + V_2] \\ i_{\max} = \dfrac{1}{2\omega L_S}[-(\pi-2\phi)nV_1 + V_2\pi] \\ \qquad = \dfrac{1}{4fsL_S}[-nV_1 + 2DnV_1 + V_2] > 0. \end{cases} \tag{2}$$

Define $m = V_2/nV_1$, then

$$i_{\max} = \frac{nV_1}{4fsL_S}[2D + m - 1]. \tag{3}$$

The maximum inductor current for $V_2 < nV_1$ is

$$i_{\max} = \frac{nV_1}{4fsL_S}[2D + |m - 1|]. \tag{4}$$

Phase-shift error is defined as the difference between actual phase shift generated by the microcontroller and the intended phase shift calculated by (1). Assume that the actual phase shift is D_1 and the calculated one is D_2. There is a phase-shift error

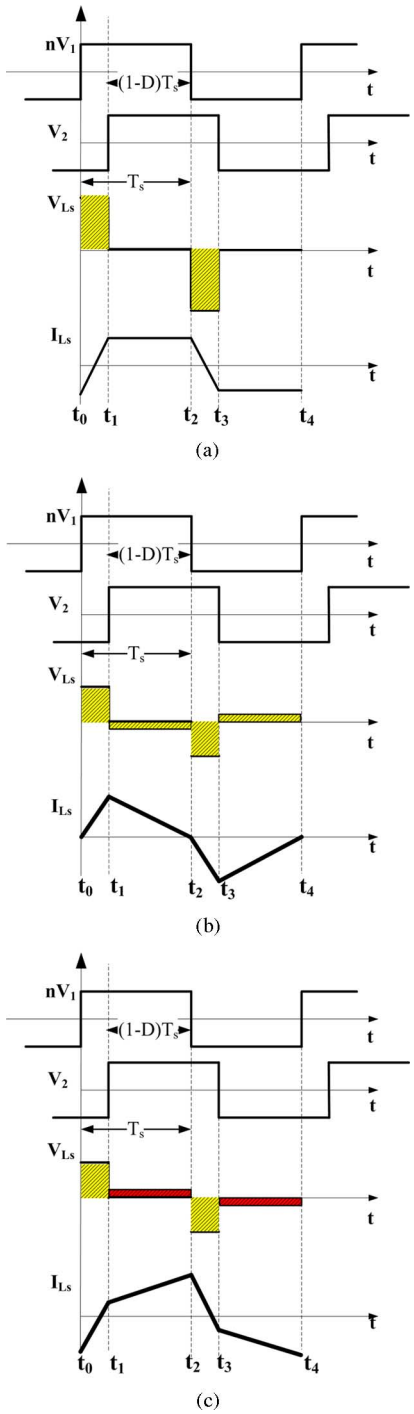


Fig. 3. Operation modes of phase-shift control under different output voltage. (a) $V_2 = nV_1$. (b) $V_2 > nV_1$. (c) $V_2 < nV_1$.

$\Delta D = D_1 - D_2$. With the intended phase-shift duty ratio D, the variation of the maximum current is

$$\Delta i_{\max}\,\% = \frac{i_{\max}(D+\Delta D) - i_{\max}(D)}{i_{\max}(D)} = \frac{2\Delta D}{2D + |m-1|} \tag{5}$$

when $m = 1$

$$\Delta i_{\max}\,\% = \frac{\Delta D}{D}. \tag{6}$$

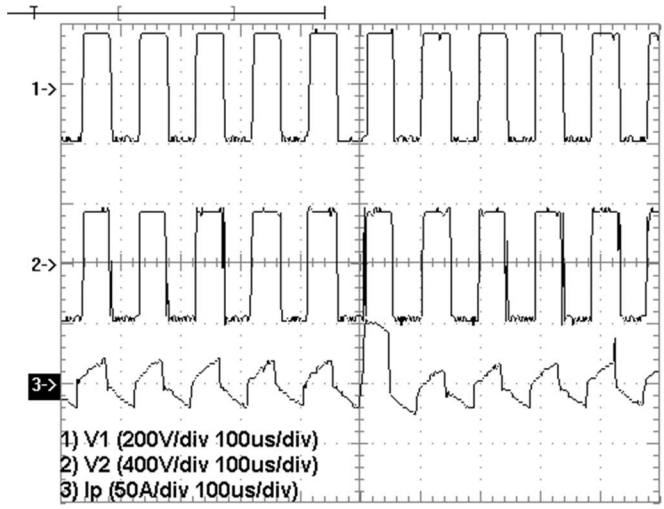


Fig. 4. Pulse sequence when current varies near $nV_1 = V_2$. (Channel 1 → V1, Channel 2 → V2, Channel 3 → Ip (primary current)).

Under light-load conditions, D is relatively small according to (1). In the present prototype system, when $P = 400$ W, $D_1 = 0.0025$; when $P = 10$ kW, $D_2 = 0.067$. The percentages of ΔD are 40% and 1.5%, respectively. That means the current variation because of phase-shift error is more severe for light-load conditions than for heavy-load conditions. Equations (5) and (6) show that the boundary condition ($m = 1$) is the most unstable operating region, especially under light-load conditions. During transients where the system shifts from $m < 1$ to $m > 1$, large current variation will appear because of phase-shift error. Simulation results are illustrated in Fig. 5, where the dotted line is the inductor current and the solid line is the voltage drop of the inductor.

Therefore, the phase-shift error is generated in the process of implementing the control algorithm and aggravated by the peripheral circuit under specific conditions.

It can be seen from Fig. 5 that only at the boundary conditions, where $V_2 = nV_1$, the current varies abruptly. In order to determine the cause of the phenomenon, we need to consider the short-time-scale transient processes, in particular, the oscillations of inductor voltage. The details of switching process are shown in Fig. 6, where G_1 stands for the gate signals of Q_1 and Q_4, G_2 for Q_2 and Q_3, G_3 for Q_5 and Q_8, and G_4 for Q_6 and Q_7.

Without the deadband, the time sequence of the gate signals should be the following.

1) Q_1 and Q_4 are turned on with Q_2 and Q_3 turned off simultaneously.
2) After a phase shift DT_S, Q_6 and Q_7 are turned off with Q_5 and Q_8 turned on.

$$\frac{Q_1}{Q_4}\ \text{ON}\ \underline{DTs}\ \frac{Q_5}{Q_8}\ \text{ON}$$
$$\frac{Q_2}{Q_3}\ \text{OFF}\ \rightarrow \frac{Q_6}{Q_7}\ \text{OFF}.$$

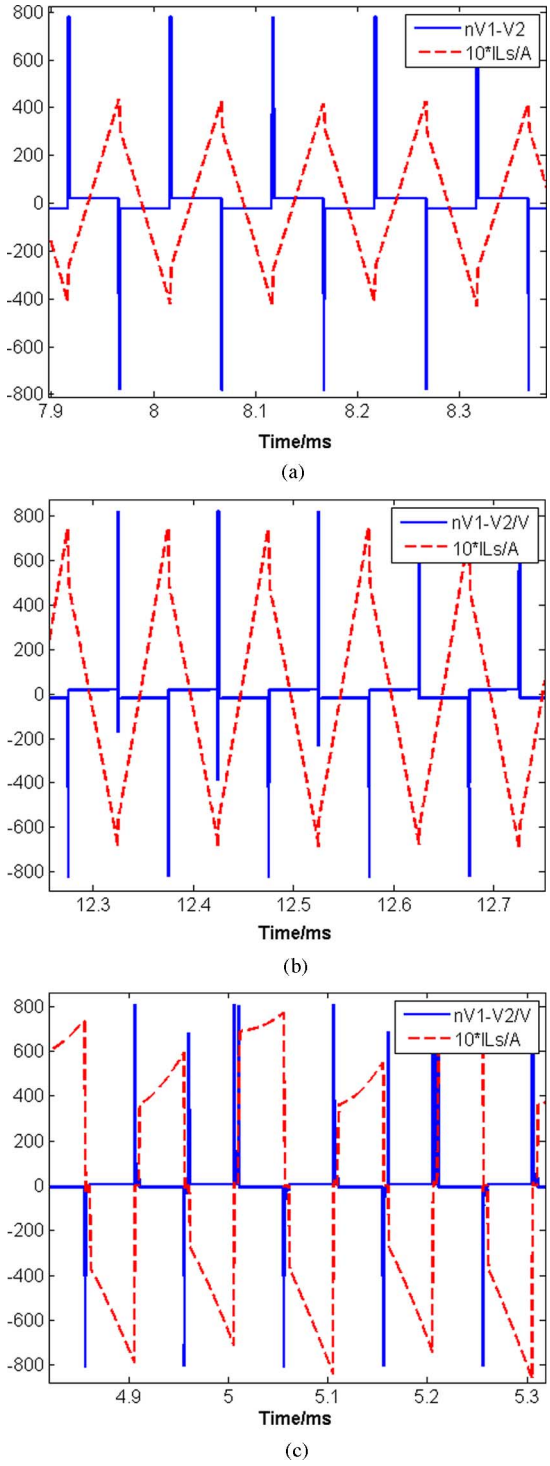


Fig. 5. Current waveforms under different operation modes. (a) $V_1 = 200$ V, $V_2 = 380$ V. (b) $V_1 = 200$ V, $V_2 = 420$ V. (c) $V_1 = 200$ V, $V_2 = 400$ V.

However, because of the deadband, the time sequence of each gate signal is changed to the following:

$$\frac{Q_2}{Q_3}\ \text{OFF}\xrightarrow{db_1}\frac{Q_1}{Q_4}\ \text{ON}\xrightarrow{\Delta}\frac{Q_6}{Q_7}\ \text{OFF}\xrightarrow{db_2}\frac{Q_5}{Q_8}\ \text{ON}$$

where db_1 and db_2 are the deadbands in the primary and secondary H-bridges, respectively. First, Q_2 and Q_3 are turned

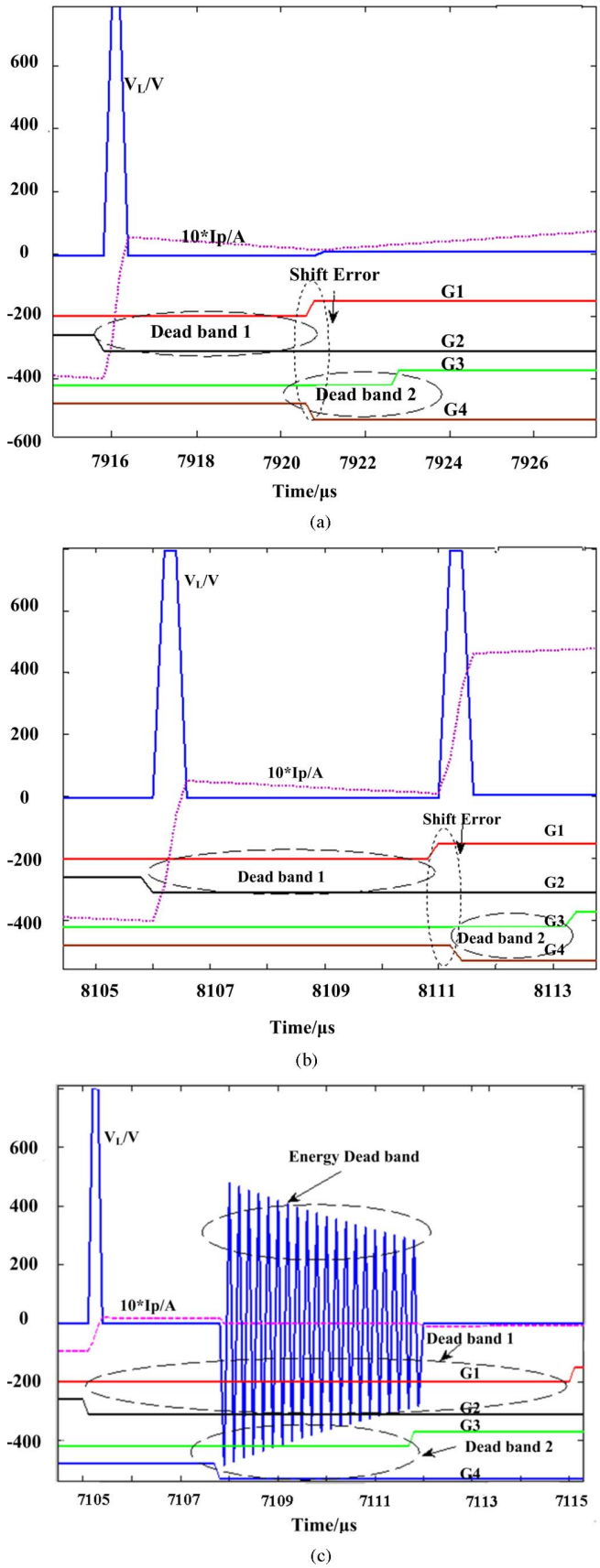


Fig. 6. Current variation caused by different time sequence of G_1–G_4. (a) Details where current is small in Fig. 5(c). (b) Details where current is large in Fig. 5(c). (c) $nV_1 = V_2$ when $P = 400$ W.

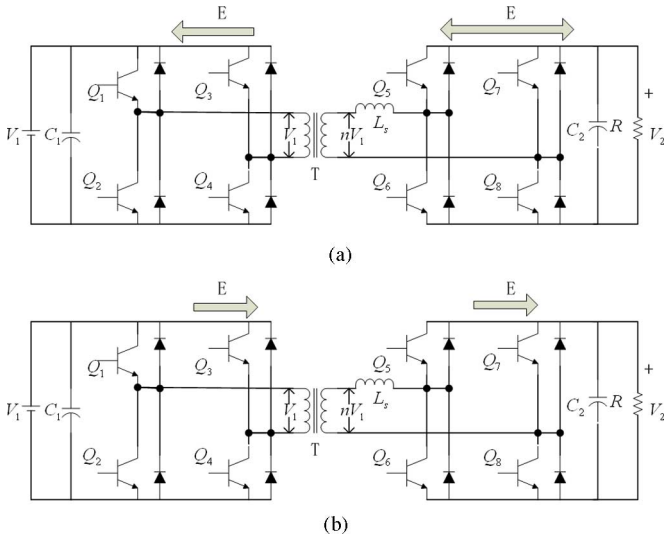


Fig. 7. Energy flows in the different stages with the consideration of deadband effects. (a) Energy flows during interval db_1. (b) Energy flows during interval ΔD and db_2.

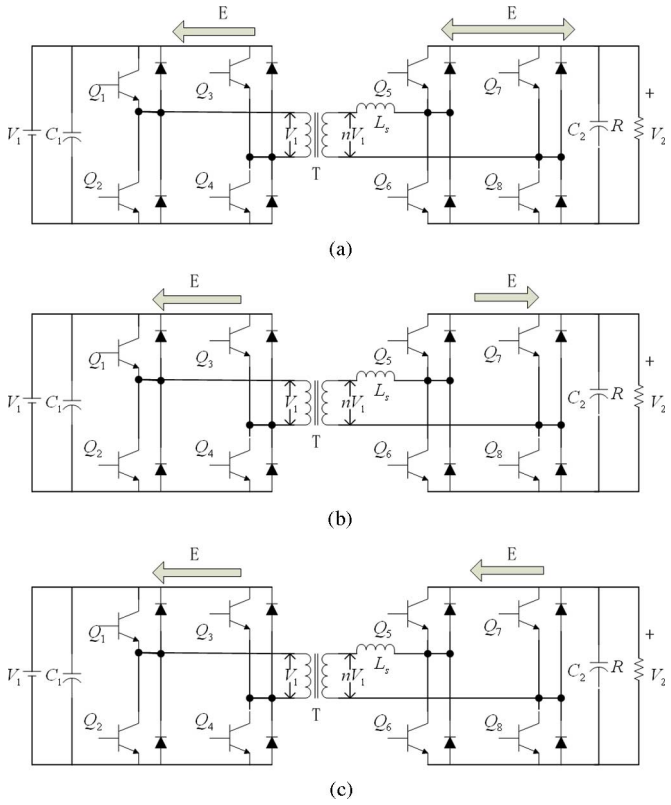


Fig. 8. Energy flow in the very light load when $\mathrm{db}_1 > \mathrm{db}_2$. (a) Energy flow during interval Δ_1. (b) Energy flow during interval db_2. (c) Energy flow during interval Δ_2.

off. After a time interval equal to db_1, Q_1 and Q_4 are turned on. After a time interval Δ, Q_6 and Q_7 are turned off. After db_2, Q_5 and Q_8 are turned on. Therefore, the time sequence with deadband is different from the time sequence without deadband. In order to clarify the actions of gate signals, we define the phase shift as the interval of $\mathrm{G}_1(\mathrm{Q}_1$ and $\mathrm{Q}_4)$ and $\mathrm{G}_3(\mathrm{Q}_5$ and $\mathrm{Q}_8)$. In Fig. 6(a) and (b), after db_1, there is a different phase-shift error ΔD between the rising edge of G_1 and the falling edge of G_4. $\Delta D = 0^\circ$ for Fig. 6(a) and $\Delta D = 3^\circ$ for Fig. 6(b).

In Fig. 6(a), ΔD is zero. Only one pulse appears in the primary voltage for 1 μs that is caused by the deadband. In Fig. 6(b), ΔD is 3°, and two pulses appear subsequently in the primary voltage. These errors are caused by PI parameters, calculating precision, or other peripheral disturbance. Although the error is not large, at low-power condition, this error could be comparable to D, which will cause a significant current variation. Some possible solutions will be discussed in Section IV.

The energy flow during the phase-shift interval is illustrated in Fig. 7. In the deadband, the whole H-bridge behaves as a rectifier. As a result, the energy could not be bidirectional. The voltage output is determined by the direction of current, and the dc bus (or the secondary) is charged. Under this condition, the system is in an undefined state.

Since the primary and secondary are equipped with different IGBTs with different current ratings, the deadtime of the two H-bridges may be different. In our system, the primary bridge is SKS30FB2CI07V12, whose maximum ratings are 850 V/65 A with an inherent deadtime $\mathrm{db}_1 = 5$ μs. The second bridge is 800 V/65 A with an inherent deadtime $\mathrm{db}_2 = 3$ μs, i.e., $\mathrm{db}_1 > \mathrm{db}_2$. These deadbands are set inherently, which could not be changed by the peripheral control circuit. If the load is very light, there will be another extreme condition, as described in Fig. 6(c). Under this condition, the time sequence of gate signals changes to the following:

$$\frac{\mathrm{Q}_2/\mathrm{Q}_3 \text{ OFF} \xrightarrow{\Delta_1} \mathrm{Q}_6/\mathrm{Q}_7 \text{ OFF} \xrightarrow{\mathrm{db}_2} \mathrm{Q}_5/\mathrm{Q}_8 \text{ ON} \xrightarrow{\Delta_2} \mathrm{Q}_1/\mathrm{Q}_4 \text{ ON}}{\overrightarrow{\mathrm{db1}}}.$$

That means, at some conditions, the turning off of Q_6 can lead the turning on of Q_5; thus, the energy flow will be different.

Here, $\mathrm{db}_1 = \Delta_1 + \mathrm{db}_2 + \Delta_2$. The energy flow diagram is illustrated in Fig. 8. It can be seen that there is always an overlap region where no energy flows from one side to the other. Energy flows only from the transformer to the two dc sides, as illustrated in Fig. 8 (b). In this condition, the energy stored in the leakage inductance will be consumed very quickly, and the current will remain at zero, which causes the oscillation of voltage across the leakage inductance, as shown in Fig. 6(c). This region could be defined as *energy deadband*, where energy flows from the inductance evenly to the primary and secondary sides of the converter in the deadband zone under specific operating conditions. No energy is transferred during this interval. Such a switching mode is very similar to the discontinuous mode in nonisolated buck or boost converters.

Energy deadband is a special phenomenon in isolated bidirectional dc–dc converters. The condition for this phenomenon to happen is light load with a small phase-shift duty ratio D, and different deadband settings for the primary and secondary bridges. Within the energy deadband, the transformer leakage inductance behaves as the energy supply, and the original power supplies serve as loads. Energy in the leakage inductor will be

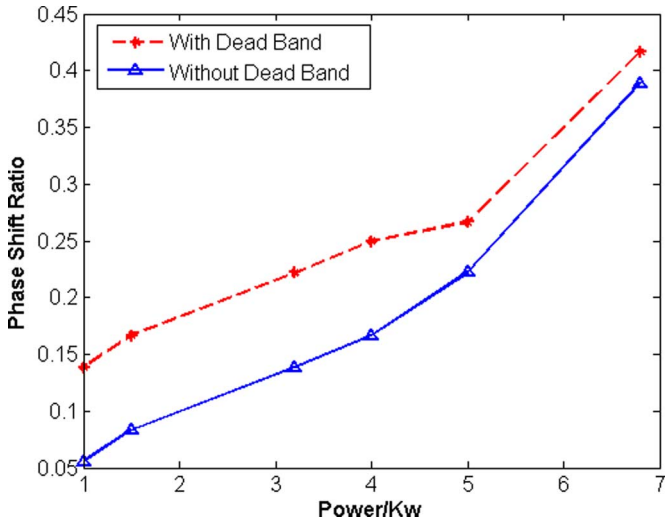


Fig. 9. Comparison of phase-shift angle in the steady state to maintain constant output voltage (simulation).

distributed to the two dc bus. The whole system is in an undefined state.

III. Deadband Effect in the Steady State

The earlier analysis on deadband effect and phase-shift error is focused on the transient processes. In fact, the deadband will not only affect the dynamic commutating process but also affect the steady state. Because of the existence of deadband, the phase-shift angle needs to be compensated in order to maintain the desired output. Fig. 9 shows the needed phase-shift ratio that is affected by deadband, where $D = 1$ corresponds to a phase-shift angle of 180°.

Fig. 10 illustrates the influences of deadband on the phase shift. Q_1–Q_8 are the gate signals for the corresponding IGBTs. The shadow area is the deadband that pushes the rising edges of gate signals backward accordingly. During these time intervals, all the IGBTs in the same H-bridge modules are turned off.

The output voltage in the deadband is determined by the direction of current. When $I(t_0) < 0$ (inside the bridge), the output voltage is nearly the same as that in the no-deadband ideal operation. When $I(t_0) > 0$, a phase shift $\Phi_{\rm db}$ is erased from the output voltage because of the deadband. To maintain the output voltage, the same as that in the ideal operation for $I(t_0) > 0$, a larger phase-shift angle is required $\phi_{\rm db} = T_{\rm deadband}{}^{*}2\pi f_S$. The actual phase shift angle is

$$\phi = \begin{cases} \phi^*, & I(t_0 \le 0) \\ \phi^* + \phi_{\rm db}, & I(t_0 > 0) \end{cases} \tag{7}$$

where ϕ^* is the ideal phase-shift angle calculated by (1): $\phi^* = 90^0 \times (1 - \sqrt{1 - 2PnV_1V_2/f_sL_s})$. Substituting (2) in (7), the actual phase-shift angle can be derived

$$\phi = \begin{cases} \frac{\pi}{2} \times \left(1 - \sqrt{1 - \frac{2PnV_1V_2}{f_sL_s}}\right), & \text{if } 1 - \sqrt{1 - \frac{2PnV_1V_2}{f_sL_s}} \ge \frac{V_2 - nV_1}{V_2} \\ \frac{\pi}{2} \times \left(1 - \sqrt{1 - \frac{2PnV_1V_2}{f_sL_s}}\right) + \phi_{\rm db}, & \text{otherwise.} \end{cases} \tag{8}$$

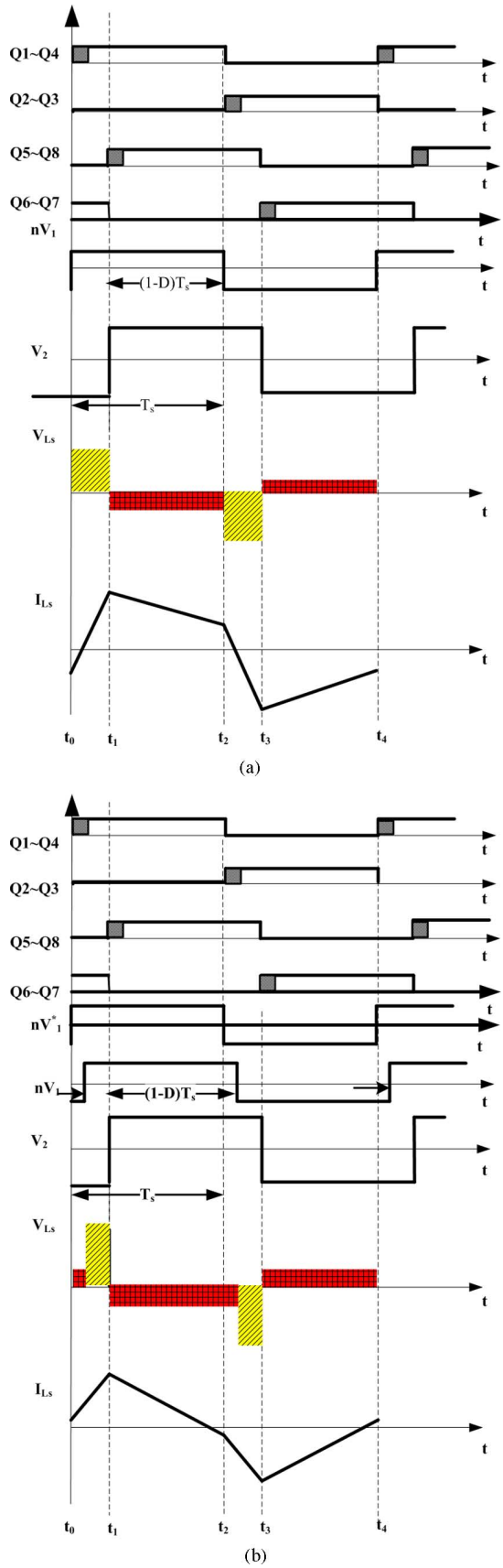


Fig. 10. Influence of deadband to the phase shift under different load conditions. (a) Phase shift under heavy load with deadband $(I(t_0) < 0)$. (b) Phase shift under light load with deadband $(I(t_0) > 0)$.

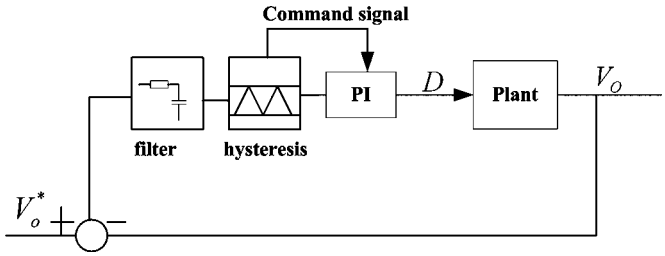


Fig. 11. Proposed schematic to erase the shift error.

From (8), if and only if power P is larger than some specific value, then the deadband influence will disappear, as illustrated in Fig. 9. This deadband compensation shift $\phi_{\rm db}$ will limit the advantage of advanced control algorithms in high-voltage and high-power converters where a large deadband is designed to guarantee the reliability and safe operation of semiconductor switches.

IV. Solutions to Mitigate the Deadband Effect and Phase-Shift Error

A. Control Algorithm Improvement

In the experimental setup, the control algorithm is a PI-based phase-shift voltage feedback control, as described in (1) and Fig. 3.

1) Feasibility of Deadband Compensation: Deadband compensation is very prevalent in inverter design to compensate the voltage distortion caused by the deadband. Most of the deadband compensation practices have to detect the direction of current and assume that during the deadband, the current will not change direction. In bidirectional dc–dc systems, current changes direction very often. The change of direction brings challenges for the deadband compensation.

2) Hysteresis for the Phase-Shifting Angle: In closed-loop voltage control, a simple PI can be used to control the phase-shift angle. A hysteresis can be set for the sampled voltage. If the voltage is within the hysteresis, the command signal is set to zero, as shown in Fig. 11. The PI modulator stops integration and will maintain the present output value. When voltage exceeds the hysteresis, the command signal is set to 1 to resume the PI control. This will erase the phase-shift error but sacrifice the sensitivity. It will also cause the static errors for the output voltage.

B. Hardware Improvement

1) Match the Turns Ratio of the High-Frequency Transformer: In order to design a 200-V/400-V isolated bidirectional dc–dc converter, the turns-ratio of the high-frequency transformer is not necessarily 1:2. In fact, a turns ratio of 1:2 will bring current variations when $m = 1$ under light-load conditions, as shown in Fig. 12, where $V_1 = 200$ V, $V_2 = 400$ V. Simulations show that a turns ratio of 1:1.5 to 1:1.8 can ensure a sufficiently large phase shift to limit deadband effect and phase-shift error.

2) Design of Leakage Inductance: To reduce the influence of phase-shift error, it is necessary to increase the leakage inductance L_s. A larger leakage inductance will improve the system

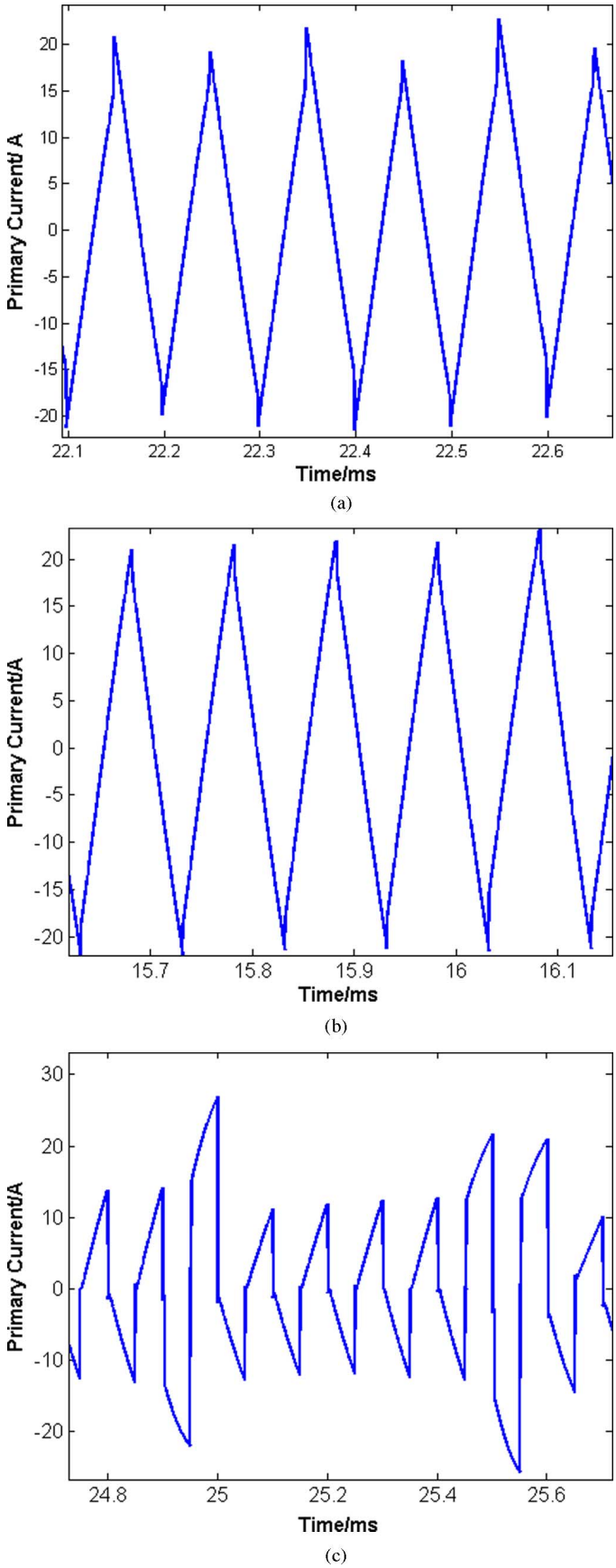
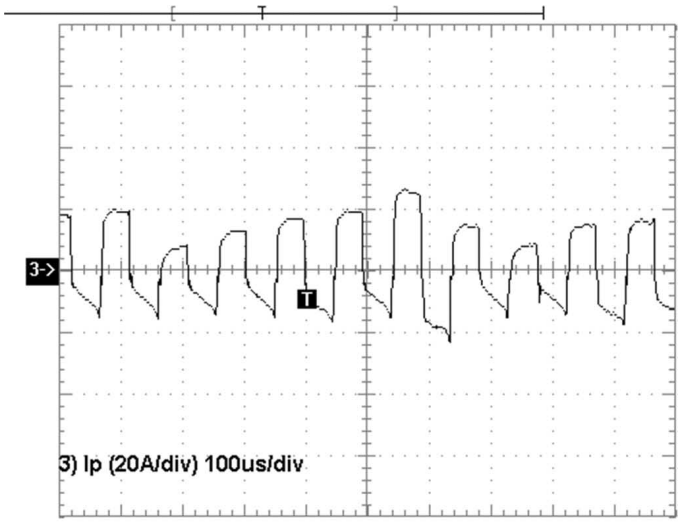
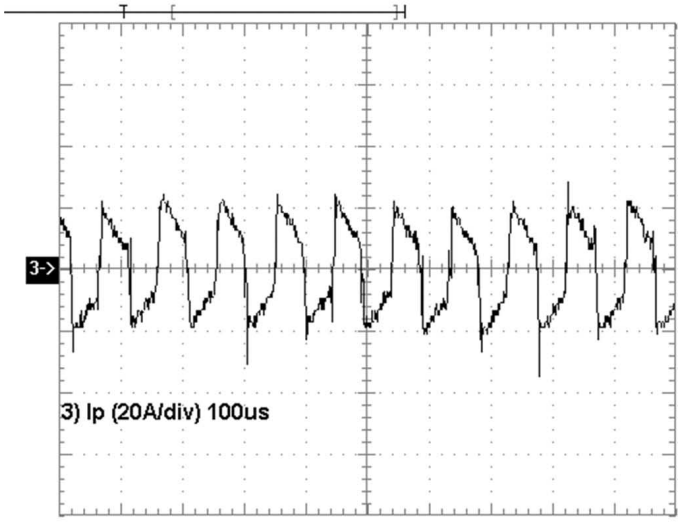


Fig. 12. Current under different turns ratio when $V_1 = 200$ V, $V_2 = 400$ V. (a) Turns ratio = 0.55:1. (b) Turns ratio = 0.47:1. (c) Turns ratio = 0.5:1.



(a)



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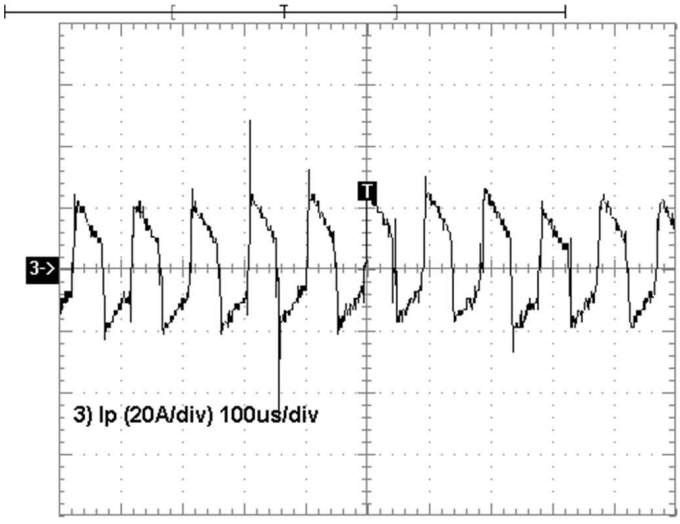

(c)

Fig. 13. Current under different inductance with $V_1 = 200$ V, $V_2 = 400$ V, and $P_o = 5.1$ kW. (a) Current under single transformers. (b) Current under series-connected transformers. (c) Current under one transformer series with another leakage inductance.

robustness. Under the same output power, a larger L_s requires a larger phase-shift angle according to (1) and (6). A larger D will decrease $i(t_0)$, as shown in (2). If $i(t_0)$ changes from positive to negative, then the deadband effect will disappear, as shown in Fig. 10. The stability of output current can also be maintained. To validate these concepts, the test platform utilizes two series-connected transformers, as well as a single transformer in series with an additional inductor to increase the leakage inductance. In the case of two transformers in series (both the primary windings and the secondary windings are in series connections), the transformation ratio n is not changed, while the leakage inductance is doubled since these two transformers are identical.

It can be seen from Fig. 13(a) that with a single high-frequency transformer, the current has long-term oscillations. In Fig. 13(b) and (c), because of the increase of leakage inductance, the current oscillations by the phase-shift errors are suppressed.

However, the leakage inductance limits the maximum output power $P_{\max}$ according to (1). Therefore, in practice, the leakage inductance should be designed to satisfy both system robustness and output power requirements.

In summary, the following design approaches can be adopted to mitigate phase-shift error.

1) Find the feasible range for the inductance with the selected turns ratio 1:n under steady-state operation by satisfying $P_{\max}$ and $I_{\max}$ with n slightly less than V_2/V_1.
2) During control algorithm design, use the hysteresis control method discussed in Section IV-A to decrease the possibility of phase-shift error.
3) The selection of inductance is further optimized through simulation by confining the voltage oscillation in an acceptable range, with a possible lowest inductance from the initial range.

V. Conclusion

The deadband effect and shift error are two important factors that affect the operation and control of high-voltage and high-power converters. Short-time-scale transient processes such as deadband effect and phase-shift error must be addressed properly in the design of high-voltage and high-power converters. Deadband effect is more significant in high-power and high-voltage dual-active-bridge (DAB)-based isolated bidirectional dc–dc converters than in conventional low-voltage and low-power converters. The relationship between power and phase-shift angle is affected by deadband. The effects of phase-shift error can be mitigated through design, control, and selection of a proper inductance. Improvements of the software and hardware design can increase robustness of the system, and move the operation mode away from the boundary condition, which is the most unstable operating region. As another short-time-scale transient, the "energy deadband" concept is defined to describe the condition where no energy flows from source to load or load to source, but only from the leakage inductance to load and sources.

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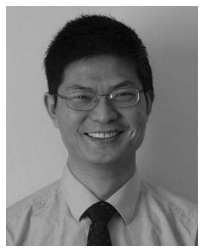

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