

Published in IET Power Electronics
 Received on 5th January 2008
 Revised on 1st March 2008
 doi: 10.1049/iet-pel:20080004



Operation, design and control of dual H-bridge-based isolated bidirectional DC–DC converter

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Abstract: The operation, design and control of an isolated bidirectional DC–DC converter for hybrid electric vehicle energy management applications are discussed. Different operation modes and boundary conditions are distinguished by phase-shift angle and load conditions. The absolute and relative output voltage ripple was derived. The dead-band effect and safe operational area are further investigated. The relations between output power and leakage inductance and switching frequency are also presented. The proposed converter was simulated and a prototype was built and tested. Experiments on the converter's steady state and transient operations validated the design and simulation.

1 Introduction

The bidirectional DC–DC converter in a hybrid electric vehicle (HEV) is a key component to manage power flow. Isolation is needed to provide safety for the equipment operating from the hybrid battery [1, 2], particularly for military and other mission critical applications [3, 4].

State-of-the-art isolated bidirectional DC–DC converters are usually based on the single-phase and full bridge topology with an isolation transformer. Fig. 1 shows the typical scheme of an isolated bidirectional DC–DC converter, which consists of a high-frequency transformer, and two H-bridges located on the primary and secondary sides of the transformer, respectively. The high-frequency transformer provides the required isolation and voltage matching between the low- and the high-voltage buses. The transformer's leakage inductance serves as the instantaneous energy storage device.

The first H-bridge provides square wave AC voltage with duty ratio of 50% to the primary winding of the high-frequency transformer. This bridge consists of four

switches Q_1 , Q_2 , Q_3 and Q_4 , commonly insulated gate bipolar transistors (IGBTs) for high power applications [5, 6]. The second H-bridge, also assembled by four switches, Q_5 , Q_6 , Q_7 and Q_8 , are connected to the secondary winding of the transformer, and operates in the boost mode by means of 'phase-shift' control. The operation is bidirectional, that is, each H-bridge can be considered as primary or secondary depending on the direction of power flow.

Previous works on isolated bidirectional DC/DC converters mainly focused on topology, control strategies and macroscopic modelling methods based on classical control theory. In [6], a three-phase high-voltage converter was presented and the transformer design with a nano-crystalline soft-magnetic material core and litz wires was discussed in detail. It also predicted the SiC utilisation in the future trend. References [7–9] depicted soft-switching techniques in DC/DC converters, which are used more and more widely to achieve high efficiency, especially in high-frequency applications. Other works pictured several feasible topologies, including the general full bridge two-level topology [10, 11], switched-capacitor

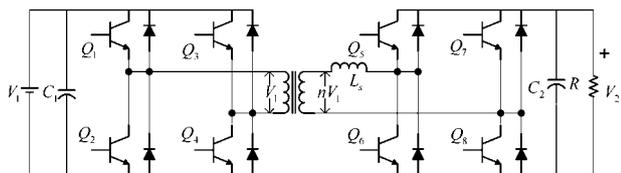


Figure 1 Isolated full-bridge bidirectional converter for HEVs

topology [12] and interleaved-buck topology [13]. On the other hand, novel control strategies, such as one-cycle control [14], and various modelling methods are carried out on isolated bidirectional DC/DC converters [15–18]. The performance characterisation under different topologies was compared in [19, 20].

Previous works lie on the macroscopic control strategies, qualitative analysis in the microscopic short-timescale phenomena [21]. Key issues, such as operation modes, voltage ripple, dead-band effect and safe operation area (SOA), have not been studied in comprehension. This paper details the different possible working conditions and presents the mathematical derivations of different operation modes. It further investigates the influential factors to the output voltage ripple, SOA design, selection of leakage inductance and switching frequency and dead-band effect. Simulations and experiments on a prototype validated the analyses.

2 Basic principle and steady-state operation

Steady-state operations of isolated bidirectional DC–DC converters have been studied in detail in previous works

[2, 4, 7]. In this paper, we complement the previous studies by distinguishing the operation modes of isolated bidirectional DC–DC converters according to the phase-shift angle, load conditions and output voltage. In this analysis, the dead-band and switching dynamics will be neglected but will be analysed in Section 4.

In the following analysis, the turns-ratio of the transformer is n , the transformer primary voltage is V_1 and the switching frequency is f_s . For the convenience of analysis, we define T_s as half switching period $T_s = 1/(2f_s)$. The duty cycle, or phase-shift, is based on half period, $D = t_{on}/T_s$. Therefore DT_s is the phase-shift between the two bridges. Further, I_{Ls} is the current of the leakage inductance of the secondary winding. The output voltage of the secondary bridge is V_2 .

2.1 Heavy load conditions

There are a number of different operation modes based on the output current with a boundary condition as illustrated in Fig. 2. Under heavy load conditions, the inductor current increases from an initial negative value $i(t_0) < 0$ at the beginning of the switching cycle, and reaches a positive value $-i(t_0)$ at the end of the half switching cycle. Six different segments emerge in each switching cycle as shown in Fig. 2a. In the following analysis, V_2 is assumed to be larger than nV_1 .

Segment 0: $[t_0, t_1]$ In this Segment, Q_1 and Q_4 of the primary bridge are turned on. Therefore V_1 and nV_1 are positive. Q_6 and Q_7 of the secondary bridge are turned on. Due to the negative current in the inductor, D_6 and

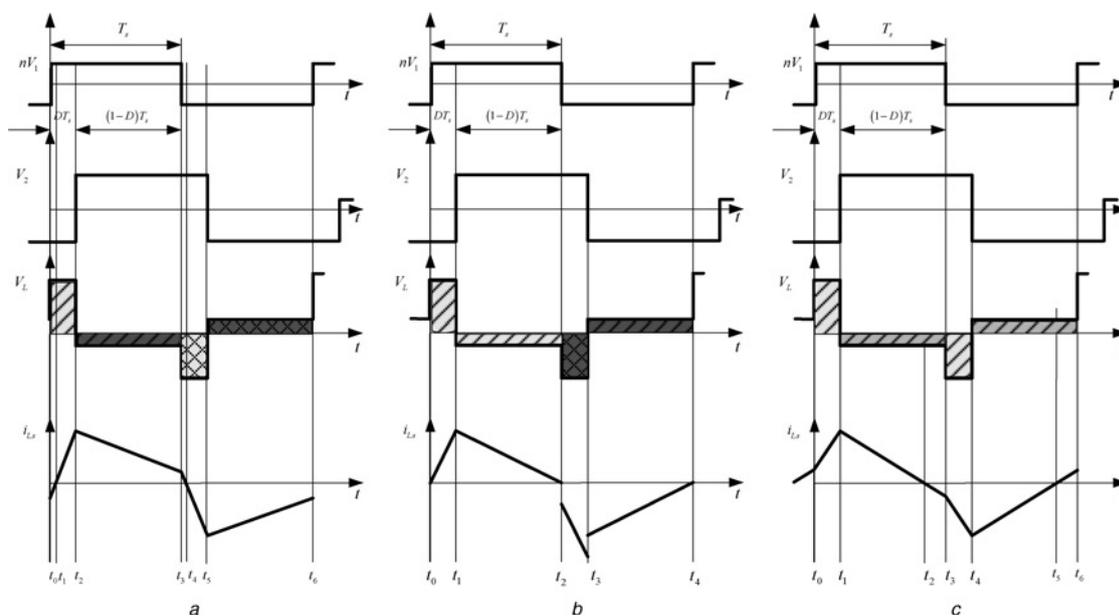


Figure 2 Typical voltage and current waveforms for $V_2 > nV_1$

- a $i(t_0) < 0$
- b Boundary conditions $i(t_0) = 0$
- c $i(t_0) > 0$

D_7 freewheel, and Q_6 and Q_7 do not conduct current. $V_{L_s} = nV_1 + V_2$. The inductor current increases linearly from a negative value. At t_1 , the inductor current reaches 0.

Segment 1: [t_1, t_2] Switches Q_1 and Q_4 of the primary bridge and Q_6 and Q_7 of the second bridge are still turned on. $V_{L_s} = nV_1 + V_2$. The current continues to increase except that the current becomes positive, therefore Q_6 and Q_7 conduct the current. The total current increment during interval [t_0, t_2] (Segments 0 and 1) is

$$\Delta I_{L_s} = \frac{DT_s}{L_s}(V_2 + nV_1) \quad (1)$$

Hence

$$i(t_2) = i(t_0) + \frac{DT_s}{L_s}(nV_1 + V_2) = I_{\max} \quad (2)$$

Segment 2: [t_2, t_3] In this Segment, Switches Q_1 and Q_4 of the primary bridge continue to be turned on, but switches Q_6 and Q_7 are turned off, and switches Q_5 and Q_8 are turned on. Diodes D_5 and D_8 freewheel because the current is positive. $V_{L_s} = nV_1 - V_2 < 0$.

The leakage inductor current increment during interval [t_2, t_3] is

$$\Delta I_{L_s} = \frac{(1-D)T_s}{L_s}(nV_1 - V_2) \quad (3)$$

Hence

$$i(t_3) = i(t_2) + \frac{(1-D)T_s}{L_s}(nV_1 - V_2) \quad (4)$$

Similar analysis could be performed for the following three segments because of the symmetry of operation.

Segment 3: [t_3, t_4] Switches Q_2 and Q_3 of the primary bridge continue to be turned on, and switches Q_5 and Q_8 are turned on. The primary voltage of the transformer, hence the secondary voltage, is reversed and the current decreases from $i(t_3)$ to zero, D_5 and D_8 freewheel.

Segment 4: [t_4, t_5] Switches Q_2 and Q_3 of the primary bridge are turned on, and switches Q_5 and Q_8 are turned on. The current decreases linearly to the negative maximum. Switches Q_5 and Q_8 conduct current. Hence the current increment in L_s in Segments 3 and 4 is

$$\Delta I_{L_s} = -\frac{DT_s}{L_s}(nV_1 + V_2) \quad (5)$$

Segment 5: [t_5, t_6] Q_5 and Q_8 are turned off, and D_6 and D_7 begin to freewheel. The current increment in L_s is

$$\Delta I_{L_s} = \frac{(1-D)T_s}{L_s}(V_2 - nV_1) \quad (6)$$

From the symmetry of the inductance current, $i(t_0) = -i(t_3)$. From (1) to (4), the initial inductor current can be obtained

$$i(t_0) = \frac{1}{4f_s L_s}[(1-2D)V_2 - nV_1] \quad (7)$$

The maximum current is

$$I_{\max} = i(t_2) = \frac{1}{4f_s L_s}[-(1-2D)nV_1 + V_2] \quad (8)$$

The above analysis of operation modes are based on the assumption that $i(t_0) < 0$, or $(1-2D)V_2 < nV_1$. If $(1-2D)V_2 = nV_1$, or

$$V_2 = \frac{1}{1-2D}nV_1 \quad (9)$$

then $i(t_0) = 0$. This corresponds to the boundary condition as shown in Fig. 2b which is very similar to the boundary condition of a non-isolated boost converter, between continuous and discontinuous mode. At this circumstance the inductor current increases from zero at the beginning of the switching cycle, and drops to zero at T_s .

From (9), it seems that V_2 will approach infinity when D reaches 0.5. But it can be seen from (7) that when $D = 0.5$, $i(t_0) = -nV_1/4f_s L_s$, therefore $i(t_0)$ will never reach zero for $D = 0.5$. The boundary can only be met when D is not equal to 0.5.

2.2 Light load condition

It can be seen from (7) that when $(1-2D)V_2 > nV_1$, then $i(t_0) > 0$. This corresponds to light load conditions. The current and voltage waveforms are shown in Fig. 2c, where the current increases from a positive value at the beginning of the cycle, and drops to a negative value at the end of the half switching cycle.

2.3 Output voltage

Equations (7)–(9) do not give the expression of the output voltage, except for the boundary condition. In order to derive an expression for the output voltage, let us start with the average current in the inductor. The average current of the leakage inductance in one half switching

cycle can be derived from Fig. 2a (note that $i(t_0) < 0$),

$$\begin{aligned} \bar{I} &= \frac{1}{2T_s} [(I_{\max} + i(t_0))DT_s + (I_{\max} - i(t_0))(1 - D)T_s] \\ &= \frac{1}{2f_s L_s} D(1 - D)V_2 \end{aligned} \quad (10)$$

The supplied power is

$$P_1 = nV_1 \bar{I} = \frac{nV_1 V_2}{2f_s L_s} D(1 - D) \quad (11)$$

Assume the load has a fixed resistance, then the output power is

$$P_o = \frac{V_2^2}{R_L} \quad (12)$$

Neglect the transformer and the switch losses, $P_1 = P_o$, therefore

$$V_2 = \frac{nV_1}{2f_s L_s} R_L D(1 - D) \quad (13)$$

and

$$I_2 = \frac{nV_1}{2f_s L_s} D(1 - D) \quad (14)$$

Equation (13) shows that, for a given switching frequency, leakage inductance and input voltage, the output voltage is proportional to the load resistance and is a function of the duty ratio (phase-shift angle). For a given load resistance, the output voltage varies with duty ratio, and reaches maximum when $D = 0.5$.

For a given duty ratio, output voltage is directly proportional to the load resistance. Therefore for a given phase-shift angle, under heavy load conditions, or $R_L < ((2f_s L_s)/D(1 - D))$, V_2 will be less than nV_1 .

When V_2 drops to less than nV_1 , the initial inductor current is confined to a negative value and the current waveforms are also different from the operations under the condition of $V_2 > nV_1$, as shown in Fig. 3. The boundary condition occurs when $S_1 = S_2 = S_3 = S_4$ in Fig. 3b, or $(nV_1 + V_2)DT_s = (nV_1 - V_2)(1 - D)T_s$. Therefore at the boundary condition

$$V_2 = nV_1(1 - 2D) \quad (15)$$

An extreme mode emerges when $nV_1 = V_2$ as shown in Fig. 3c, where the inductor current will remain constant during time interval $[DT_s, T_s]$.

It can also be seen from (14) that the output current is proportional to the duty ratio (phase-shift angle). This may be used to analyse conditions where the output voltage needs to be maintained as constant, and the current can be controlled through the phase-shift angle.

The cases shown in Figs. 2 and 3 can be validated by experiments, as shown in Fig. 4 where the operation modes for $nV_1 > V_2$, $nV_1 < V_2$ and $nV_1 = V_2$ are shown.

2.4 Output power

Substitute (13) to (11), the output power P_o can be obtained

$$P_o = \left(\frac{nV_1}{2f_s L_s} \right)^2 D^2(1 - D)^2 R_L \quad (16)$$

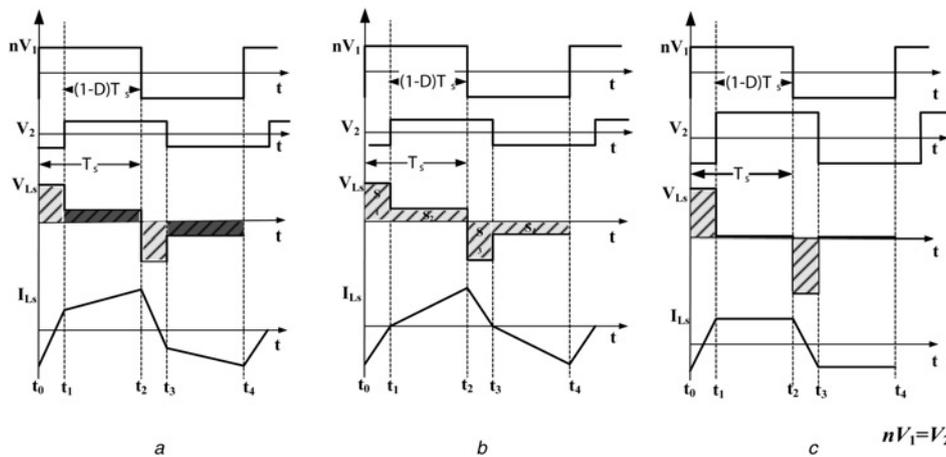


Figure 3 Typical voltage and current waveforms for $V_2 < nV_1$ and $V_2 = nV_1$

- a Common mode
- b Boundary mode
- c Extreme mode, $nV_1 = V_2$

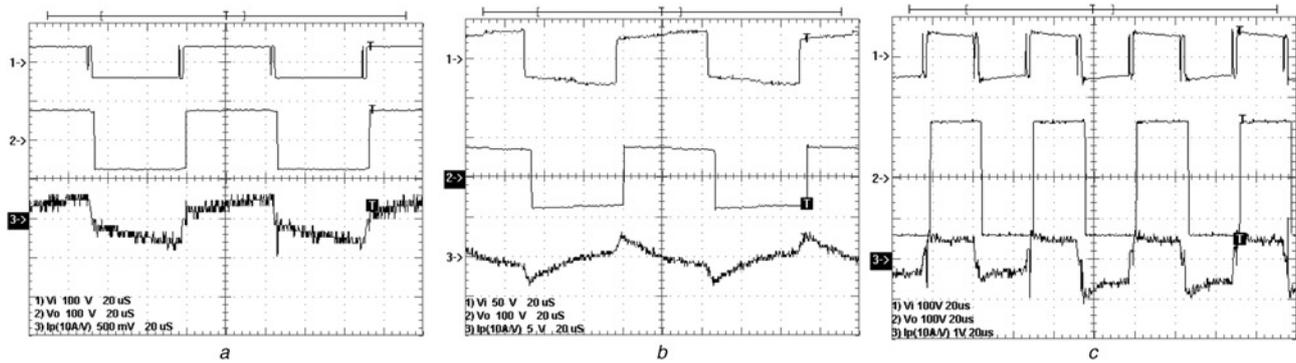


Figure 4 Different steady-state operation modes

Channel 1 $\rightarrow V_1$, Channel 2 $\rightarrow V_2$, Channel 3 \rightarrow primary current of transformer

a $nV_1 > V_2$

b $nV_1 < V_2$

c $nV_1 = V_2$

From (11) and (16), the output power always has the maximum values when and only when $D = 1/2$ whether for a fixed resistance R_L or a constant output voltage V_2 .

When the system is in the voltage closed-loop control mode $V_2 = \text{constant}$, then decreasing R_L will result in the output power increasing since the output power is inversely proportional to R_L as shown in (12). To maintain V_2 as a constant, it can be seen from (13) that D has to be adjusted accordingly: $D(1 - D) \propto 1/R_L$ for a given V_1 . For fixed V_1 and V_2 , the output power reaches maximum at $D = 0.5$ as shown in (11). At this condition, $R_L = R_C = 8f_s L_s (V_2/nV_1)$.

Further decrease of $R_L < R_C$ will result in the output voltage of the system to collapse and enter the open loop at $D = 0.5$, and V_2 cannot be maintained as a constant. Output voltage V_2 and output power P_o will decrease, and are both proportional to R_L as shown in (13) and (16).

Consider (7) and (16), When $D \in (0, 1/2]$, if V_1 , V_2 are kept constants (closed loop control), with the increase of D , the power will increase accompanying the decrease of the initial current $i(t_0)$. Hence the absolute value and the sign of $i(t_0)$ represent the load condition. The less the inductor current $i(t_0)$, the higher is the output power.

Under open-loop control, that is, for a given D , with the increase of load resistance, V_2 and P_o will increase according to (13) and (16). At the same time, the initial current increases according to (7) due to the increase of V_2 . Hence the relations between initial current and the output power are very different in the open- and closed-loop operation of the converter.

In order to validate the theoretical analysis, a simulation model was set up with $V_1 = 200$ V, $n = 2$, $L_s = 120$ μ H. In Figs. 5a and 5b, with the increase of power, the initial current decreases from positive value to negative value. In Figs. 5c and 5d, the variation of initial current is opposite. These are in good agreement with the earlier analysis.

Fig. 6 shows the test results on the bench setup for $V_2 = 80$ V, $f_s = 20$ kHz. The test results have demonstrated functionality of the setup and supported the above theories. It can be seen from Fig. 6 that when the resistance decreases, in order to maintain a constant output voltage, the phase-shift increases, whereas the initial current $i(t_0)$ decreases. It validates the previous theory and simulation.

The maximum output power is also a function of L_s and f_s . Increase the leakage inductance L_s will decrease the current impact to IGBTs but will reduce the capability of the maximum output power of the converter as shown in (16). This will be further discussed in Section 4 of this paper.

3 Voltage ripple

The above switch-modes are inherently nonlinear, which will cause voltage ripple on the output capacitor. The capacitor current is the combination of the inductor current I_L and the load current I_o at different operation modes. For example, in Fig. 2, the capacitor current can be written as

$$\begin{aligned} i_C &= -(I_o + i_L), & 0 \leq t \leq DT_s \\ i_C &= i_L - I_o, & DT_s \leq t \leq T_s \end{aligned} \quad (17)$$

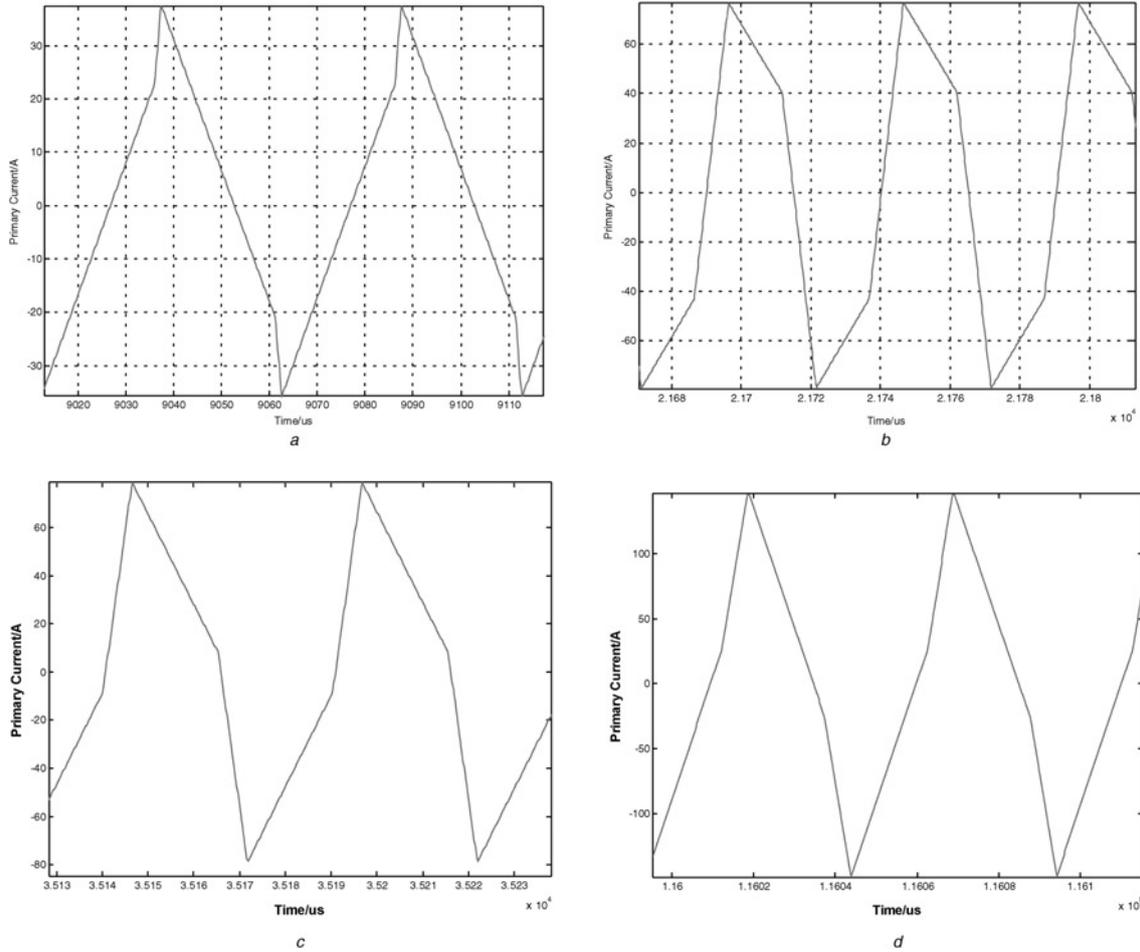


Figure 5 Simulation power, the current and phase-shift angle

- a $V_2 = 600 \text{ V}$, $R = 200 \ \Omega$, $P = 1.8 \text{ kW}$
- b $V_2 = 600 \text{ V}$, $R = 40 \ \Omega$, $P = 9 \text{ kW}$
- c $D = 1/8$, $R = 60 \ \Omega$, $P = 8.2 \text{ kW}$
- d $D = 1/8$, $R = 100 \ \Omega$, $P = 13.6 \text{ kW}$

The capacitor current is shown in Fig. 7, where at $t = t_1 + \Delta_2$, $I_{Ls} = I_o$, or $I_C(t_1 + \Delta_2) = 0$, that is

$$I_{\max} + \frac{nV_1 - V_2}{L_s} \Delta_2 = I_o \quad (18)$$

therefore

$$\Delta_2 = \frac{I_{\max} - I_o}{V_2 - nV_1} L_s \quad (19)$$

On the basis of the energy conservation, $P_1 = P_o$, or $nV_1 \bar{I} = V_2 I_o$. Substitute (11) for P_o , the output current can be obtained

$$I_o = \frac{nV_1}{2f_s L_s} D(1 - D) \quad (20)$$

The voltage ripple is

$$\Delta V_2 = \frac{1}{C} \int_{DT_s}^{DT_s + \Delta_2} (i_{Ls}(t) - I_o) dt = \frac{\Delta_2}{C} \frac{I_{\max} - I_o}{2} \quad (21)$$

Substitute (18), (19) and (20) to (21), the voltage ripple can be derived

$$\left\{ \begin{aligned} \Delta V_2 &= \frac{[V_2 + (2D^2 - 1)nV_1]^2}{32f_s^2 L_s C (V_2 - nV_1)} \\ &= \frac{[D(1 - D)R_L - 2(1 - 2D^2)f_s L_s]^2 nV_1}{64f_s^3 L_s^2 [D(1 - D)R_L - 2f_s L_s]} \frac{1}{C} \\ \Delta V_2 \% &= \frac{\Delta V_2}{V_2} \\ &= \frac{[D(1 - D)R_L - 2(1 - 2D^2)f_s L_s]^2}{32f_s^2 L_s C [D^2(1 - D)^2 R_L^2 - 2f_s L_s D(1 - D)R_L]} \end{aligned} \right. \quad (22)$$

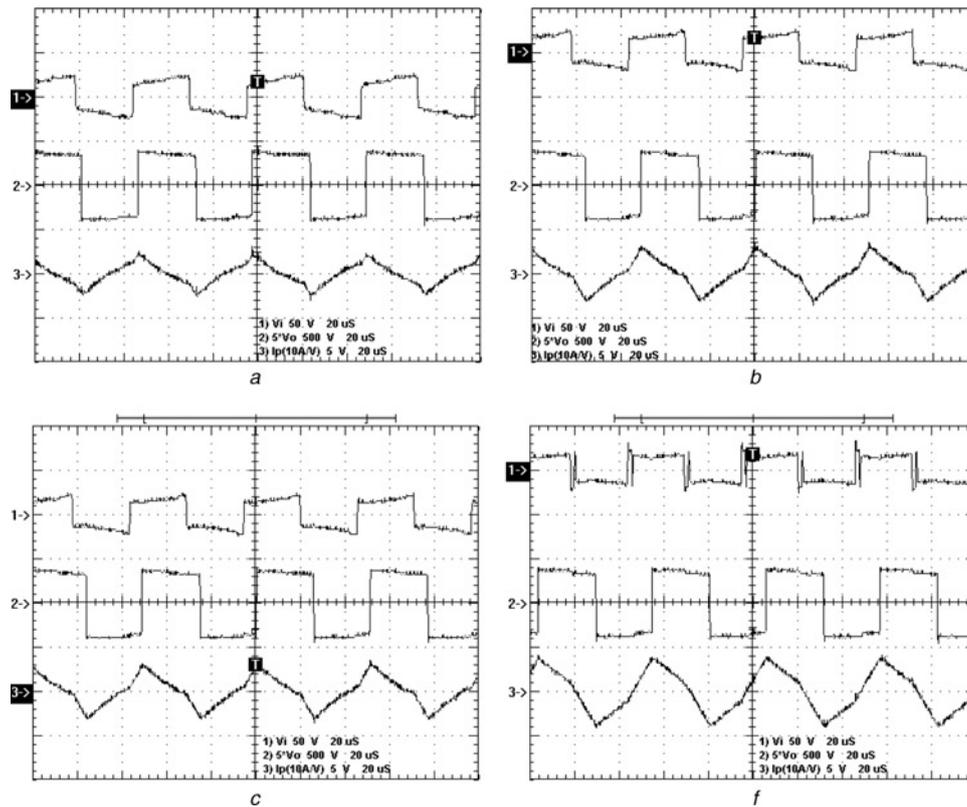


Figure 6 Initial current under different load conditions

- a No load
- b $R_L = 66 \Omega$
- c $R_L = 33 \Omega$
- d $R_L = 22 \Omega$

Therefore the voltage ripple is a function of D , R and nV_1 . This expression is applicable to both open- and close-loop controls. The condition of (22) is $V_2 > nV_1$, which implies $D(1 - D)R_L > 2f_s L_s$. From (22), it is easy to see that ΔV_2 is directly proportional to nV_1/C . In order to further study

the influential factors, the voltage ripple under different conditions is shown in Fig. 8.

From Fig. 8a, the absolute voltage ripple decreases when R_L decreases under a given D , and the ripple

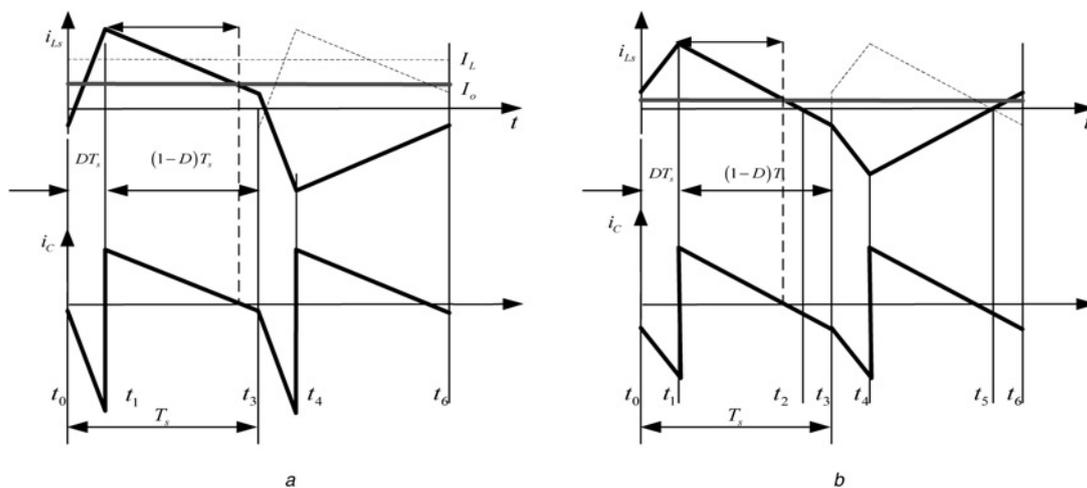


Figure 7 Current ripple in the capacitor

- a $i(t_0) < 0$
- b $i(t_0) > 0$

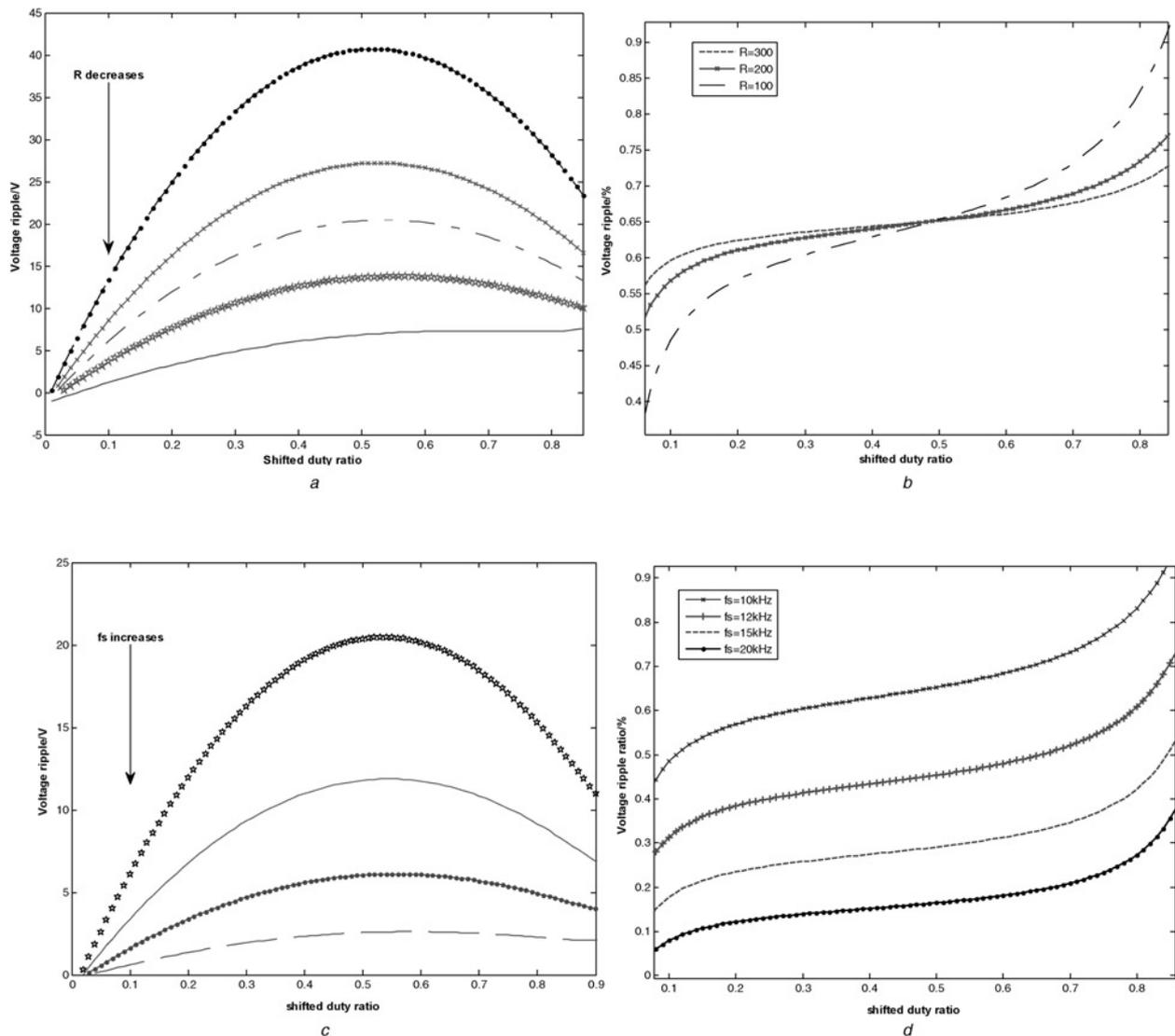


Figure 8 Voltage ripple under different operations (simulation)

- a Voltage ripple as a function of D and R_L
 b Voltage ripple (%) as a function of D and R_L
 c Voltage ripple as a function of D and f_s
 d Voltage ripple (%) as a function of D and f_s

reaches maximum at $D = 0.5$. However, in Fig. 8b, the relative ripple is an increasing function of D and only reaches the maximum when $D = 1$. All the curves cross at $D = 0.5$.

When $D < 0.5$, high resistance will result in a high ripple under a fixed D . When $D > 0.5$ the absolute ripple decreases with D for a given load resistance, but the relative ripple increases with D .

From Figs. 8c and 8d, increasing the switching frequency is beneficial to limit both the absolute ripple and the relative ripple of the output voltage.

4 Special issues in the DC–DC converter design

4.1 Dead-band effect

To avoid the shoot-through of the bridge in the commutating process, a dead-band is inserted between the interlocked switches in the same bridge. Dead-band is very crucial to guarantee the reliability of the system operations. However, dead-band will cause waveform distortion and other unexpected short-timescale phenomena as shown in Fig. 9a.

During the dead-band, all of the four semiconductors in the primary H-bridge, Q_1 – Q_4 will be turned off. In

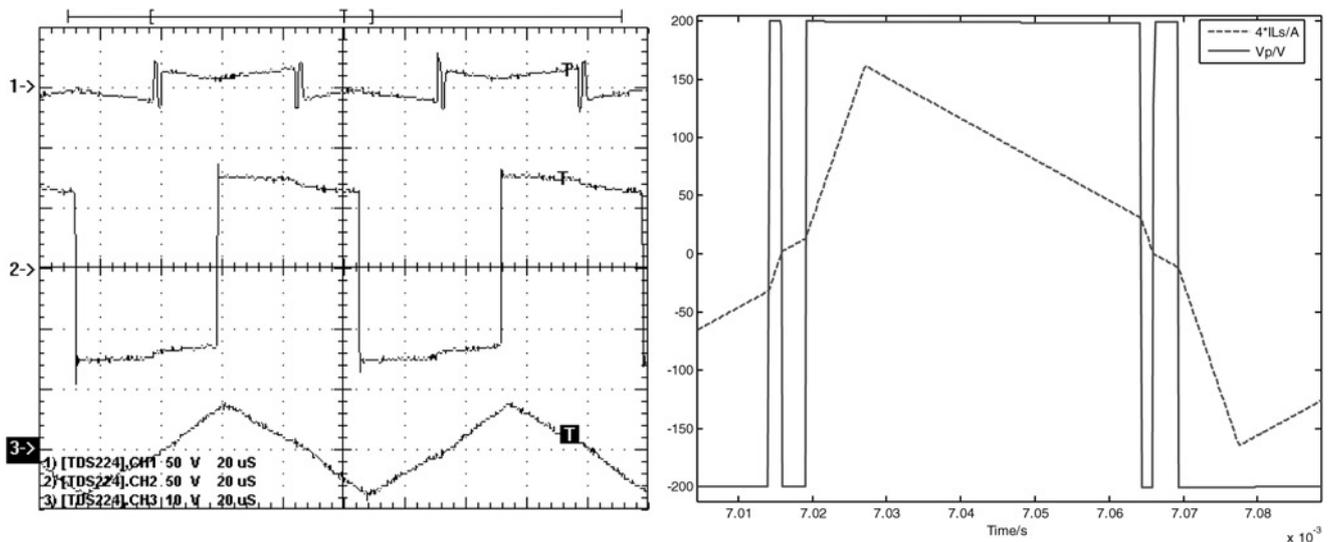


Figure 9 Dead-band effect on the primary voltage waveforms

a Experiment

b Simulation

Channel 1 \rightarrow V_1 , Channel 2 \rightarrow V_2 , Channel 3 \rightarrow I_p (primary current)

this interval the inductor current oscillates near zero and eventually causes the polarity of output voltage vary dramatically. Therefore the spurs in the primary voltage shown in Fig. 9a will appear. Simulation also validated this analysis as shown in the Fig. 9b. The spurs emerging in the primary voltage are caused by the change of current direction in the dead-band. This spur will not deteriorate the system operation, but sometimes the frequent variation of voltage waveforms may bring electromagnetic interference (EMI).

The output voltage in the dead-band is determined by the current direction, when $i(t_0) < 0$ (inside the bridge) the primary output voltage is nearly the same as that in the no-dead-band ideal operation. When $i(t_0) > 0$ a phase-shift Φ_{db} is erased from the output voltage due to the dead-band. Hence for $i(t_0) > 0$, in order to maintain the same output power as in the ideal operation, a compensation of Φ_{db} in phase-shift is required, where $\phi_{db} = T_{deadband} * 2\pi f_s$.

4.2 SOA design

SOA design for the DC–DC converter is also very important to guarantee that the IGBTs and other components such as the isolated transformer are in safe operation at any circumstance. The design of L_s and f_s is a trade off. With fixed f_s , a larger L_s will decrease the maximum output power while small L_s will bring high current impact on the transformer and IGBTs. For a given L_s , the current amplitude decreases with the increase of f_s .

Fig. 10 shows the simulation results of peak current as a function of output power, frequency and leakage

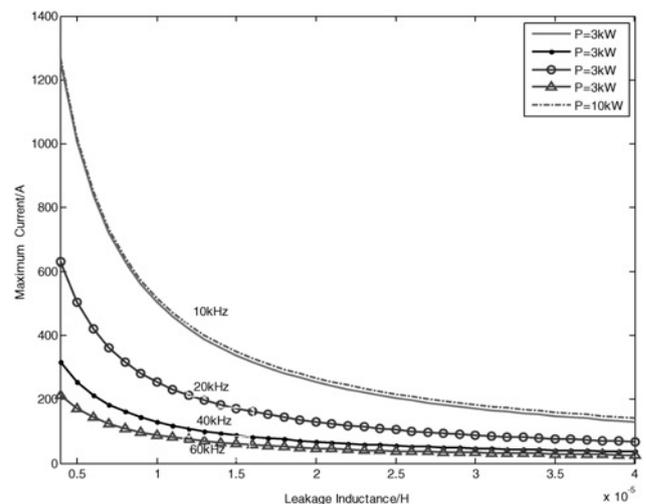


Figure 10 Maximum current against L_s and f_s

inductance. It shows that the peak current increase very little when the output power increases from 3 to 10 kW (top two curves for $f_s = 10$ kHz). With the increase of switching frequency, the peak current drops significantly. The peak current also decreases with the leakage inductance.

The maximum f_s is limited by the inherent characteristics of silicon devices. The absolute maximum switching frequencies of most commercial IGBTs will not exceed 20 kHz. Real designs should focus on the inductance design. On the other hand, the present utilised IGBT modules mostly have good voltage-blocking capability but relatively lower current endurance. For example, the IGBT, B2C110V12 by

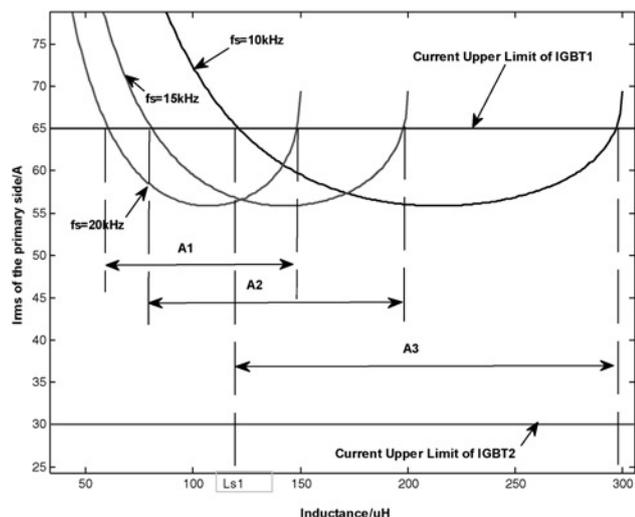


Figure 11 SOA design

Semikron could withstand voltage of 1200 V but only 30 A current (in root-mean-square value or rms) at the most.

The rms current in the primary side of the transformer could be calculated according to Fig. 2 and expressed as

$$I_{\text{rms}} = 2 \sqrt{i(t_0)i_{\text{max}}(2D - 1) + \frac{(i(t_0) + i_{\text{max}})^2}{3}(1 - D) + \frac{(i_{\text{max}} - i(t_0))^2}{3}D} \quad (23)$$

The relationships between the primary rms current and the inductance under different switching frequency are calculated and shown in Fig. 11 for a 10 kW converter design. The figure also shows the current limitations of two different IGBT devices, one at 30 A and the other at 65 A.

If the IGBT is operated at 10 kHz, inductance must be between 120 and 300 μH (range A1 in Fig. 11). Only IGBT₂ can satisfy the 10 kW power requirement. If $L_s < 120\mu\text{H}$, the current will exceed the threshold. If $L_s > 300\mu\text{H}$, the maximum output power will be smaller than 10 kW. If the IGBT is operated at 15 or 20 kHz, then the leakage inductance must be further reduced to meet the 10 kW power requirement (range A2 and A1 in Fig. 11, respectively).

5 Conclusion

The operation, design and control of isolated bidirectional DC–DC converter are complex and comprehensive from semiconductor selection to peripheral circuit design, and

from long-timescale steady-state operation to short-timescale pulsed power phenomena. This paper analysed the operation principles and various switching modes of the dual H-bridge-based DC–DC converter, and derived the expressions of voltage ripple. The relations between voltage, current and power are derived and supported by the experiments of the prototype. Some special issues in the real applications are discussed and tested by experiments, including dead-band effect in the transient and steady state, and SOA for the 10 kW prototype converter.

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