A Novel Five-Level Neutral Point Clamped (NPC) Single-Phase Inverter

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***Abstract*— A novel five-level inverter based on neutral point clamped (NPC) and switched-capacitor technology is proposed in this article. The proposed inverter uses six unidirectional switches, two bidirectional switches, and three capacitors. The inverter has voltage-boosting capability, allowing it to increase the voltage by a gain factor of 1.5. Other features of the proposed inverter include its ability to manage the return current, which enables the control of reactive power. Consequently, the proposed inverter effectively controls reactive power, even at very low power factors. The switched capacitor has charging and discharging currents at the switching frequency, which helps to reduce the impact of current spikes in this converter. The design of the passive components within the proposed inverter is provided. To demonstrate the pros and cons of the proposed inverter compared to other inverters, a comparative analysis is presented. Finally, to verify the performance of the proposed inverter, the experimental results for a 2-kW system with high efficiency are provided.**

***Index Terms*— Neutral point clamped (NPC), single-stage system, switched-capacitor technology, voltage boosting.**

I. Introduction

MULTILEVEL inverters (MLIs) have emerged as a promising alternative to conventional two-level inverters, significantly improving output waveform quality and increasing power ratings [1], [2], [3], [4]. Among traditional multilevel topologies, the neutral point clamped (NPC) [5] and flying capacitor (FC) [6] converters have been widely adopted due to their single dc-link design, which simplifies the feeding circuits, including transformers and rectifiers. However, these conventional topologies present notable challenges, especially as the number of levels increases. For instance, a five-level NPC (5L-NPC) inverter requires multiple clamping diodes, leading to increased power losses, while a five-level FC (5L-FC) inverter demands a large capacitance, making the design bulky and costly. Furthermore, regulating the dc-link voltages in NPC converters and balancing floating capacitor voltages in FC converters necessitate additional auxiliary circuits and complex modulation techniques [7], [8].

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The introduction of the three-level NPC inverter in 1979 marked a major advancement in power electronics, laying the foundation for the MLI concept [9]. Since then, MLIs have been widely adopted in industrial applications [10], [11]. To enhance efficiency, compactness, and voltage levels, researchers have pursued various improvements to traditional NPC inverters. One method to increase the number of voltage levels is to vertically extend the topology by adding more series-connected dc-link capacitors. However, this approach results in a higher component count and increased implementation complexity. To address these drawbacks, advanced topologies, such as active-NPC (ANPC) inverters, have been developed, replacing clamping diodes with power switches to reduce conduction losses and integrate floating capacitors for increased voltage levels [12], [13], [14].

Transformerless inverters are another area of focus, particularly for grid-connected photovoltaic (PV) systems, where reducing leakage current is essential. Traditional approaches, such as PWM bipolar modulation, stabilize the common mode voltage (CMV) but result in high dv/dt, necessitating large filters and leading to increased power losses. Conversely, unipolar PWM modulation reduces dv/dt, decreases filter size, and minimizes power losses, but it causes CMV fluctuations at the switching frequency. NPC and ANPC inverters mitigate these issues by connecting both the dc source midpoint and the grid neutral point, maintaining a constant CMV, and improving system performance [13], [14], [17], [18].

This article proposes a novel five-level inverter that integrates NPC and switched-capacitor technologies to address the limitations of traditional NPC and ANPC inverters. The proposed inverter features eight switches, including two four-quadrant switches, and incorporates a switched-capacitor circuit to achieve voltage boosting with a gain of 1.5. This design significantly reduces the required input voltage by 66.6% while maintaining the same output specifications, enabling direct grid connection without an additional dc–dc converter. Moreover, the inverter ensures inherent voltage balance for the capacitors, eliminating the need for complex balancing mechanisms and enhancing reliability, particularly for battery-based energy storage systems (BESSs) operating in the 300–400-V range.

Additionally, in the proposed topology, the switched capacitor charges and discharges at the switching frequency, which allows for a significant reduction in capacitor charging current amplitude by selecting an appropriate switching frequency. This feature contrasts with conventional switched-capacitor

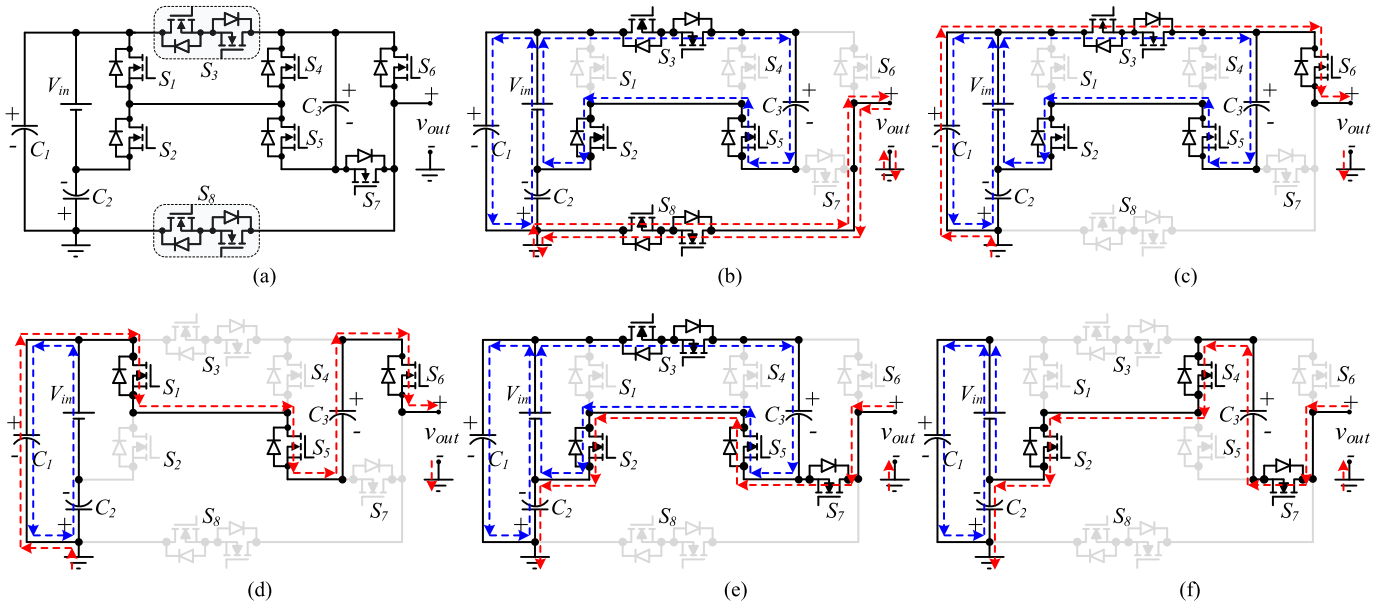

Fig. 1. Proposed five-level inverter and its operating modes. (a) Proposed topology, (b) first mode, $v_{out} = 0$ V, (c) second mode, $v_{out} = +0.5V_{in}$, (d) third mode, $v_{out} = +1.5V_{in}$, (e) fourth mode, $v_{out} = -0.5V_{in}$, and (f) fifth mode, $v_{out} = -1.5V_{in}$.

converters, where capacitors charge and discharge at a fraction of the grid frequency, leading to higher current amplitudes and greater stress on components. Moreover, the bidirectional capability of the inverter makes it highly suitable for BESS applications, allowing efficient power flow in both directions for charging and discharging operations.

The remainder of this article is organized as follows. Sections II and III describe the proposed inverter topology and its operating modes. Section IV presents the circuit analysis and passive component design. Section V provides a comparative evaluation of the proposed inverter against the existing topologies. Finally, the experimental results and conclusions are given in Sections VI and VII.

II. Proposed 5L-NPC-Based Single-Phase Inverter

The proposed NPC inverter is illustrated in Fig. 1(a). This inverter, which is of the NPC type, can produce five voltage levels at the output terminal (v_{out}). Two levels of the output voltage correspond to the positive half cycle, two levels correspond to the negative half cycle, and the zero level is common to both the positive and negative half cycles. The inverter uses ten switches and three capacitors, with switches S_3 and S_8 being bidirectional or four-quadrant, capable of blocking voltage bilaterally. As a result, a total of eight PWM signals and gate drivers are required. Capacitors C_1 and C_2, or the NPC capacitors, are located at the input of the inverter, with each charged to half of the input voltage. Capacitor C_3 is also charged according to the input voltage. The proposed inverter has voltage-boosting capability, allowing it to increase the input voltage by 1.5 times. Because the negative terminal of the load or grid is connected to the midpoint of the input capacitors, the proposed inverter maintains a constant common-mode voltage and reduces or eliminates leakage current in PV systems. Therefore, it can be stated that the proposed inverter is suitable for renewable energy systems (RESs), especially PV applications. Additionally, the inverter's ability to handle reverse current enables it to supply nonunity power factor loads in grid-forming mode. In the grid-following mode, it controls the reactive power injected into the grid.

In battery energy storage systems, a power electronic-based interface capable of transferring power in both directions is required to charge batteries from the grid or inject energy from the batteries into the grid. The proposed inverter, with its bidirectional capability, serves as a suitable interface for battery energy storage systems. During low grid load conditions, batteries can be charged from the grid, and during peak load conditions, energy can be returned to the grid.

III. Operating Modes of the Proposed Inverter

The operating modes of the proposed inverter are illustrated in Fig. 1(b)–(f). In these figures, the path of output power is shown by red lines, while the charging path of the capacitors is shown by blue lines. Additionally, paths with no current are shown in a dim color. Each of the capacitors C_1 and C_2 is charged to half of the input voltage, while capacitor C_3 is charged to the full input voltage. Capacitor C_1 provides output power during the positive half cycle, and capacitor C_2 provides output power during the negative half cycle. Meanwhile, capacitor C_3 provides output power during both half cycles.

To create zero voltage at the output of the inverter, the equivalent circuit in Fig. 1(b) is used. To generate a $+0.5V_{in}$ voltage at the output terminal, capacitor C_1 is employed, as shown in Fig. 1(c). For generating a $+1.5V_{in}$ voltage, the series connection of capacitors C_1 and C_3 is utilized, as depicted in Fig. 1(d). Similarly, to produce a $-0.5V_{in}$ voltage at the output terminal, capacitor C_2 is used, as shown in Fig. 1(e). Finally, to produce a $-1.5V_{in}$ voltage at the output, the series connection of capacitors C_2 and C_3 is used, as illustrated in Fig. 1(f).

Table I details the switching operations, showing how each switch is turned on and off and how capacitors are charged

TABLE I
SWITCHING PATTERN OF THE PROPOSED INVERTER

V_{out}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	C_1	C_2	C_3
±0	0	1	1	0	1	0	0	1	↑	↑	↑
+0.5V_{in}	0	1	1	0	1	1	0	0	↓	↑	↑
+1.5V_{in}	1	0	0	0	1	1	0	0	↓	↑	↓
-0.5V_{in}	0	1	1	0	1	0	1	0	↑	↓	↑
-1.5V_{in}	0	1	0	1	0	0	1	0	↑	↓	↓

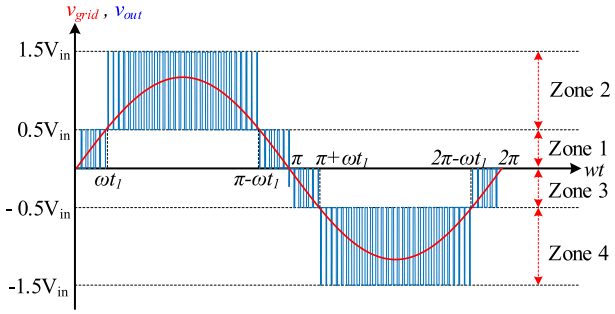

Fig. 2. Five-level output voltage of the proposed inverter and grid voltage.

and discharged. In this table, the number "0" indicates that the switch is off, while the number "1" indicates that the switch is on. The arrow "↑" denotes the charging state of the capacitor, and the arrow "↓" denotes the discharging state of the capacitor.

IV. Duty Cycle Calculation and Design Guidelines of Passive Components

A. Duty Cycle Calculation

Since the proposed inverter produces different voltage levels at the output terminal, it has different duty cycles in each operating zone. The five-level output voltage of the inverter, along with the load or grid voltage, is shown in Fig. 2. As observed in Fig. 2, the proposed inverter has four operating zones: Zones 1 and 2 correspond to the positive half cycle, while Zones 3 and 4 correspond to the negative half cycle.

In Zone 1, the output voltage of the inverter varies between 0 and $+0.5V_{\text{in}}$, while in Zone 2, it varies between $+0.5V_{\text{in}}$ and $+1.5V_{\text{in}}$. Similarly, in Zone 3, the output voltage ranges from 0 to $-0.5V_{\text{in}}$, and in Zone 4, it ranges from $-0.5V_{\text{in}}$ to $-1.5V_{\text{in}}$. The duty cycle of the inverter is identical in Zones 1 and 3, as well as in Zones 2 and 4. The voltage and current of the load at unity power factor are expressed as follows:

$$v_{\text{Load}}(t) = V_{\text{Load,max}} \sin(\omega t) \tag{1}$$

$$i_{\text{Load}}(t) = I_{\text{Load,max}} \sin(\omega t) \tag{2}$$

where ω is the angular frequency of the fundamental output, $V_{\text{Load,max}}$ is the peak load voltage, and $I_{\text{Load,max}}$ is the peak load current.

By applying the volt-second balance rule to the output inductor in Zones 1 and 2 and simplifying the result, the duty cycles of the proposed inverter are expressed as follows:

$$d_1(t) = \frac{v_{\text{Load}}(t)}{0.5V_{\text{in}}} = \frac{V_{\text{Load,max}}}{0.5V_{\text{in}}} \cdot \sin(\omega t); \quad 0 \le t < t_1 \tag{3}$$

$$d_2(t) = \frac{v_{\text{Load}}(t)}{V_{\text{in}}} - 0.5 = \frac{V_{\text{Load,max}}}{V_{\text{in}}} \cdot \sin \omega t - 0.5; \quad t_1 \le t < \frac{\pi}{\omega} - t_1. \tag{4}$$

Time t_1 can be calculated by the following equation:

$$t_1 = \frac{1}{\omega} \sin^{-1}\left(\frac{0.5V_{\text{in}}}{V_{\text{Load,max}}}\right). \tag{5}$$

Table II shows the duty cycle of each switch in different operating zones. According to this table, the duty cycle for each switch during a complete grid cycle can be observed. This information is highly useful for implementing PWM pulses within the microcontroller.

B. Output Filter Design

For the proposed five-level inverter, an *LC*-type filter is employed. Therefore, it is essential to determine the values of L_f and C_f. The output inductor value reaches its maximum at $\omega t = \pi/2$. To compute the inductor value, the current integral equation for Zone 2 is formulated as follows:

$$i_{Lf}(t) = \frac{1}{L_f} \int_0^t V_{Lf} dt + i_{Lf}(0); \quad t_1 \le t < \frac{\pi}{\omega} - t_1. \tag{6}$$

By substituting (4) into (6) and simplifying, the value of the output inductor is determined as follows:

$$L_f = \frac{1}{\Delta i_{Lf} \cdot f_S}\left(2V_{\text{Load,max}} \sin(\omega t) - \frac{V_{\text{Load,max}}^2}{V_{\text{in}}} \cdot \sin^2(\omega t) - \frac{3}{4} \cdot V_{\text{in}}\right). \tag{7}$$

Finally, the value of the inductor is calculated as follows, considering the maximum ripple of the inductor current:

$$L_f = \frac{1}{\Delta I_{Lf,\max} \cdot f_S}\left(2V_{\text{Load,max}} - \frac{V_{\text{Load,max}}^2}{V_{\text{in}}} - \frac{3}{4} \cdot V_{\text{in}}\right). \tag{8}$$

To calculate the capacitance value of the output filter capacitor, the voltage integral for the output capacitor is formulated. Considering the maximum voltage ripple for the filter capacitor, its value is determined as follows:

$$C_f = \frac{\Delta i_{Lf}}{8 f_S \cdot \Delta v_{\text{Load}}} \tag{9}$$

$$C_f = \frac{2V_{\text{Load,max}} - \frac{V_{\text{Load,max}}^2}{V_{\text{in}}} - \frac{3}{4} \cdot V_{\text{in}}}{8 f_S^2 \cdot L_f \cdot \Delta V_{\text{Load,max}}}. \tag{10}$$

C. Calculation of Capacitors C_1–C_3

In the proposed inverter, each capacitor C_1 and C_2 carries half of the output current. The maximum voltage ripple occurs at $\omega t = \pi/2$. By applying the voltage integral for C_1 and C_2 and simplifying the expression, their values for maximum voltage ripple are determined as follows:

$$C_1 = C_2 = \frac{I_{\text{Load,max}}}{2\omega \cdot \Delta V_{C1,\max}}. \tag{11}$$

TABLE II
DUTY CYCLE OF SWITCHES IN DIFFERENT OPERATION ZONES

	Switches	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Positive half cycle	Zone1	0	1	1	0	1	$d_1(t)$	0	1-$d_1(t)$
	Zone2	$d_2(t)$	1-$d_2(t)$	1-$d_2(t)$	0	1	1	0	0
Negative half cycle	Zone3	0	1	1	0	1	0	$d_1(t)$	1-$d_1(t)$
	Zone4	0	1	1-$d_2(t)$	$d_2(t)$	1-$d_2(t)$	0	1	0

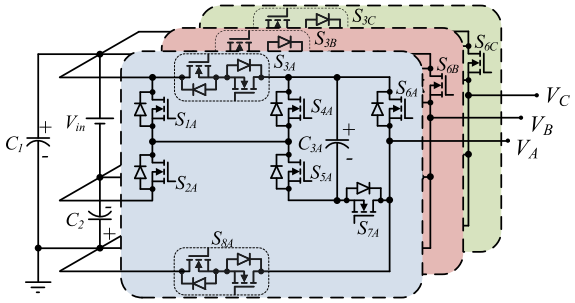

Fig. 3. Three-phase configuration of the proposed NPC-based five-level inverter.

Capacitor C_3 is a switched capacitor that charges according to the input voltage. Based on the operating modes of the proposed inverter, this capacitor charges in all modes and discharges only during the $v_{\text{out}} = \pm 1.5V_{\text{in}}$ modes. By applying the voltage integral for capacitor C_3, its value can be determined based on the maximum voltage ripple as follows:

$$\Delta v_{C3}(t) = \frac{1}{C_3}\int_0^{d_2 T_S} i_{\text{Load}} dt = \frac{i_{\text{Load}} \cdot d_2}{C_3 \cdot f_S} \tag{12}$$

$$C_3 = \frac{I_{\text{Load,max}} \cdot \left(\frac{V_{\text{Load,max}}}{V_{\text{in}}} - 0.5\right)}{\Delta V_{C3,\text{max}} \cdot f_S}. \tag{13}$$

The voltage stress on the switches in the proposed inverter is calculated using the following equations:

$$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{S5} = V_{S6} = V_{S7} = V_{\text{in}} \tag{14}$$

$$V_{S8} = 1.5V_{\text{in}}. \tag{15}$$

The proposed five-level inverter can be extended to a three-phase inverter, as shown in Fig. 3. In this figure, the input source and capacitors C_1 and C_2 are shared across all three phases, and each phase has its separate module.

V. COMPARISON STUDY

To demonstrate the advantages of the proposed inverter compared to other inverters, a comparison is necessary. Since the experimental results of the proposed inverters in the references were obtained under different power levels and conditions, a direct comparison using the results from those papers is not feasible. For a fair comparison, the inverters must be simulated under identical conditions. In this section, MATLAB Simulink software is used to compare the proposed inverter with other inverters. The input voltage for all inverters is set to 270 V, and the output voltage of the inverter before filtering is 400 V. Additionally, the load voltage is set to 230 V rms, the switching frequency is 30 kHz, and the output power is 1 kW. For the NPC capacitors C_1 and C_2, a value of 1.45 mF is used, and for capacitor C_3, a value of 90 μF is employed. With these capacitor values, the voltage ripple percentage is 10% for C_1 and C_2 and 3% for C_3.

TABLE III
VALUES OF THE PASSIVE COMPONENTS IN THE COMPARED INVERTERS

Topologies	Values of passive components
[12]- 2023	C_1=C_2=0.6mF, C_F=20μF, L_{boost}=1mH, C_{boost}=1mF, L_f=1mH, C_f=1μF
[13]- 2020	C_1=C_2=0.55mF, C_F=3.2mF, L_f=1mH, C_f=1μF
[14]- 2019	C_1=C_2=0.55mF, C_{F1}=3.2mF, C_{F2}=3.2mF, L_f=1mH, C_f=1μF
[15]- 2019	C_1=C_2=1.25mF, C_F=2.5mF, L_{boost}=1mH, C_{boost}=1mF, L_f=1mH, C_f=1μF
[16]- 2020	C_1=C_2=0.58mF, C_F=20μF, L_{boost}=1mH, C_{boost}=1mF, L_f=1mH, C_f=1μF
[17]- 2023	C_1=C_2=0.55mF, C_{F1}=3.2mF, C_{F2}=3.2mF, L_f=1mH, C_f=1μF
[18]- 2022	C_1=C_2=0.6mF, C_{F1}=3.2mF, C_{F2}=3.2mF, L_f=1mH, C_f=1μF
Proposed	C_1=C_2=1.45mF, C_3=90μF, L_f=1mH, C_f=1μF

The output filter inductor value for all inverters is set to 1 mH, and the output filter capacitor value is 1 μF. The internal resistance of all inductors and capacitors is 0.1 Ω. The internal resistance of all switches and diodes is 0.08 Ω, and the forward voltage drop of the diodes is 0.7 V. The inverters presented in [12], [15], and [16] have a voltage gain of one. To ensure that the comparison is conducted under identical conditions, a boost converter is used at the input of these inverters. The input voltage of the boost converter is 270 V, and the output voltage is 400 V. The boost converter operates at a frequency of 30 kHz. For the boost converter inductor, a value of 1 mH is used, and for the output capacitor of the converter, also known as the dc bus capacitor, a value of 1 mF is employed. The same voltage ripple percentage is considered for the NPC capacitors and the FCs in other inverters, with the obtained values shown in Table III.

To effectively compare inverters based on the volume of passive components, the total maximum energy stored in the inductors and capacitors can be calculated. This is determined using the following equations:

$$\text{Vol}_L \cong \text{Tot.\_}W_L = 0.5 \times \sum_{i=1}^{N_L} L_i \cdot I_{L,\text{max}}^2 \tag{16}$$

$$\text{Vol}_C \cong \text{Tot.\_}W_C = 0.5 \times \sum_{i=1}^{N_C} C_i \cdot V_{C,\text{max}}^2 \tag{17}$$

TABLE IV
COMPARISON TABLE BETWEEN THE PROPOSED INVERTER AND OTHER INVERTERS

Topologies	N_S	N_D	N_C	N_L	V_{IN}	V_{OUT}	Boosting factor	Tot. W_C (J)	Tot. W_L (mJ)	TSV (P.U.)	Conduction Losses (W)	THD of V_{Load} %	f_S for the same THD
[12]- 2023	9	1	4	2	400	400	1	105.6	69.2	7	23.5	1.62	26.4 kHz
[13]- 2020	9	-	3	1	270	400	1.5	126.66	19.2	5.4	33	1.13	18.8 kHz
[14]- 2019	10	-	4	1	270	400	1.5	243.3	19.2	7.425	26	1.12	18.8 kHz
[15]- 2019	11	1	4	2	400	400	1	180	69.2	9	41	1.57	26 kHz
[16]- 2020	9	1	4	2	400	400	1	104.8	69.2	8	23	1.61	26.3 kHz
[17]- 2023	8	2	4	1	270	400	1.5	243.3	19.2	8.07	28	1.1	18.5 kHz
[18]- 2022	6	2	4	1	270	400	1.5	244.21	19.2	6.07	27	1.98	34.5 kHz
Proposed Converter	10	-	3	1	270	400	1.5	29.7	19.2	7.4	18.7	1.78	30 kHz

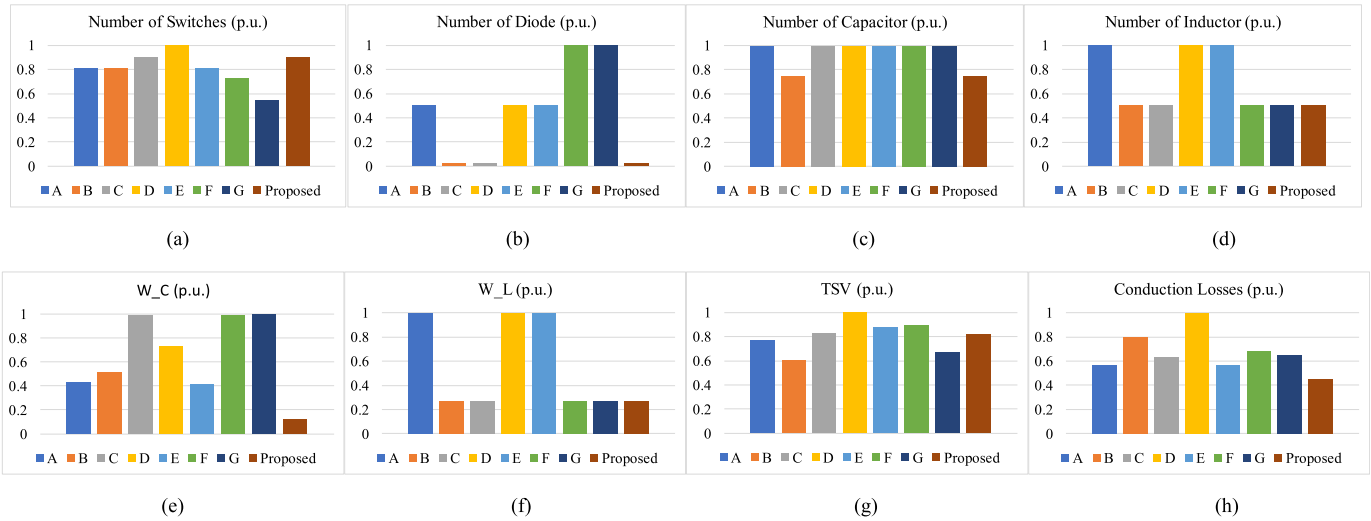

Fig. 4. Comparison between the proposed inverter and other inverters. A = [12], B = [13], C = [14], D = [15], E = [16], F = [17], and G = [18]. (a) Number of switches, (b) number of diodes, (c) number of capacitors, (d) number of inductors, (e) maximum stored energy in capacitors *W_C*, (f) maximum stored energy in inductors *W_L*, (g) TSV, and (h) conduction losses.

where Tot._W_L represents the total maximum energy stored in the inductors of the converter, while Tot._W_C denotes the total maximum energy stored in the capacitors. N_L and N_C are the numbers of inductors and capacitors, respectively. Additionally, $I_{L,\max}$ is the maximum current through the inductors, and $V_{C,\max}$ is the maximum voltage across the capacitors. To determine the total standing voltage (TSV) in converters, (18) is employed, as shown in the following:

$$\text{TSV} = \frac{\sum_{i=0}^{N_D+N_S} V_i}{V_{\text{OUT}}} \tag{18}$$

where N_S and N_D represent the number of switches and diodes in the converters, respectively. Table IV provides a comparison between the proposed inverter and other inverters. The comparison parameters include the number of switches, diodes, inductors, capacitors, the total maximum energy stored in inductors and capacitors, TSV, boosting factor, conduction losses, total harmonic distortion (THD) of the load voltage, and switching frequency to have the same output voltage THD.

The inverter presented in [12] has one fewer switch compared to the proposed inverter and a slightly lower TSV. However, it requires one additional diode, capacitor, and inductor. It lacks voltage-boosting capability, has a larger volume of energy storage components, and exhibits higher conduction losses.

The inverter presented in [13] has one fewer switch than the proposed inverter and a lower TSV. However, the energy stored in its capacitors is significantly higher than that of the proposed inverter, and it also exhibits high conduction losses.

The inverter presented in [16] has one fewer switch compared to the proposed inverter but requires an additional diode, capacitor, and inductor. It lacks voltage-boosting capability and has a larger volume of energy storage components. This inverter also exhibits higher TSV and conduction losses compared to the proposed inverter.

While the inverters shown in [17] and [18] have fewer switches than the proposed inverter and the TSV of the inverter in [18] is lower than that of the proposed inverter, they both require two additional diodes and one additional capacitor. The energy stored in the capacitors of these inverters is significantly higher than that of the proposed inverter, and they also exhibit higher conduction losses. The lower THD of the output load voltage in the structures [13], [14], [17] is attributed to their seven-level output voltage before filtering. This results in higher energy storage in the capacitors, leading to increased conduction losses. Fig. 4 presents a bar graph comparing the proposed inverter with other inverters. The data shown in this figure are directly derived from the comparison table.

TABLE V
EXPERIMENTAL PARAMETERS

Element	Type
Input voltage (V_{in})	270V DC
Output voltage peak value (V_{out})	311V
Switching frequency	32kHz
Output power (P_{out})	2kW
Power switches	C2M0080120D
C1 & C2	3300 µF
C3	940 µF
Output filter inductor (L_f)	335 µH
Output filter capacitor (C_f)	1 µF
Gate Driver	ACPL-H342
Isolated DC-DC converter	MGJ2D121505SC
Microcontroller	TMS320F280049M

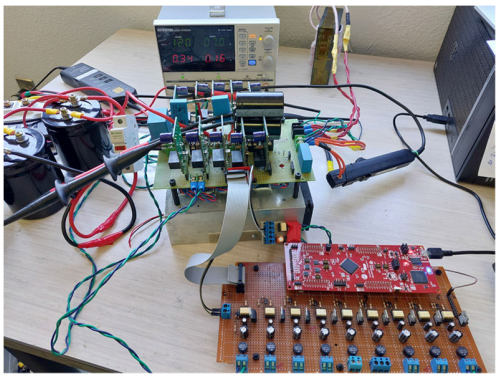

Fig. 5. Experimental setup for file-level proposed inverter.

VI. EXPERIMENTAL RESULTS

The performance and capabilities of the proposed converter are validated by the experimental results presented in this section. Table V details the parameters of the active and passive components used in the experimental setup, illustrated in Fig. 5. The TMS320F280049 microcontroller generated PWM pulses and controlled the converter. A Chroma 62100H-600 programmable dc power supply served as the input voltage source (PV Simulator).

The converter's efficiency at different operating points was measured using a YOKOGAWA WT1800 power analyzer. Experimental waveforms were captured with a Tektronix MDO4054-3 oscilloscope, and voltages and currents were measured using a Tektronix TCPA300 current probe and a Tektronix TPA-BNC voltage probe. In Fig. 6(a), the five-level inverter output voltage (V_{OUT}), capacitor C_3 voltage, output load voltage, and output load current are shown in order from top to bottom. In this figure, the input voltage is 270 V, and the output voltage is 220-V rms with a peak of 311 V. The output power is 2 kW. From Fig. 6(a), it can be observed that capacitor C_3 is charged to 270 V, which is equal to the input voltage. In Fig. 6(b), the output voltage of the inverter before the filter, the voltage of capacitor C_3, the voltage of capacitor C_1, and the voltage of capacitor C_2 are displayed. The input voltage is 270 V, and the power is 2 kW. According to this figure, capacitors C_1 and C_2 are each charged to half of the input voltage, which is 135 V for each capacitor. Additionally, capacitor C_3 is charged to the full input voltage. Fig. 6(c) shows the five-level output voltage, capacitor C_3 voltage, output load voltage, and capacitor C_3 current. In this figure, the input voltage is 270 V, and the power is 2 kW.

To illustrate the voltage stress on the switches in the inverter, Fig. 7(a) and (b) is provided. Fig. 7(a) shows the voltage stress of switches S_1 through S_4, while Fig. 7(b) displays the voltage stress of switches S_5 through S_8. Since switches S_3 and S_8 are four-quadrant switches, their voltage stress is bidirectional, whereas the rest of the switches exhibit unidirectional voltage stress. According to Fig. 7(a) and (b), the voltage stress of all switches is equal to the input voltage, except for switch S_8, which experiences a voltage stress equal to the output voltage. Specifically, switches S_1 through S_7 have a voltage stress equal to V_{in}, while switch S_8 has a voltage stress equal to $1.5V_{\mathrm{in}}$.

Since the proposed inverter has the capability to reverse the output current, it can effectively feed nonunity power factor loads. Fig. 7(c) illustrates the performance of the proposed inverter under nonunity power factor conditions. To create a phase difference between the voltage and current of the output load, a series connection of a 40-μF capacitor and an inductor is used with the output load. From this figure, it can be observed that there is a significant phase difference between the voltage and current, exceeding 80°. This indicates that the proposed inverter can handle loads with very low power factors.

Handling transition conditions and maintaining output voltage stability during step changes in output power are crucial parameters for the proposed inverter. To evaluate these capabilities, step changes in output power were applied to the proposed inverter, and the results are shown in Fig. 8. In Fig. 8(a), power changes are applied at $\omega t = 1.5\pi$, with the output power increasing from 1.14 to 1.6 kW. The figure shows that the output voltage, load voltage, and capacitor C_3 voltage remain constant before and after the power change, with only the load current range increasing. Fig. 8(b) illustrates more drastic power changes, where the output power increases from zero to 2 kW at $\omega t = 0.5\pi$. The figure indicates that the output voltage, load voltage, and capacitor C_3 voltage remain stable before and after the load change, while the output current ramps up from zero to its peak value.

Fig. 8(c) shows the transition from nominal power to zero power. The figure demonstrates that the proposed inverter remains stable throughout this process. To demonstrate the experimental efficiency of the proposed inverter, Fig. 9 is presented. This figure includes the power supply, oscilloscope, and power analyzer used to measure the inverter's efficiency. The efficiency of the converter is depicted at three different output power levels. Fig. 9(a) shows the experimental efficiency of the inverter at the output power of 1.14 kW, in which the efficiency value is measured as 98.27%. Fig. 9(b) shows the efficiency of the inverter at the output power of 1.59 kW, which is equal to 97.82%. Finally, in Fig. 9(c), the efficiency of the inverter has been measured at the output power of

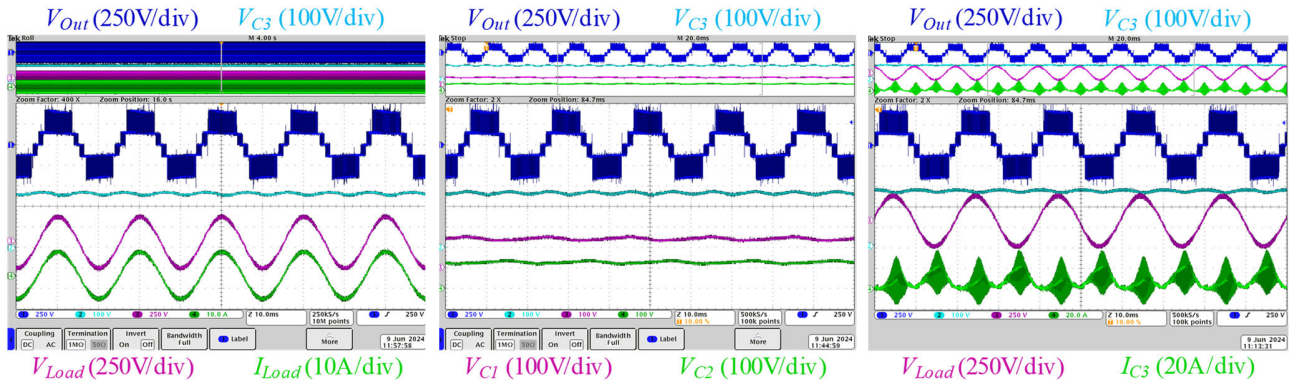

Fig. 6. Experimental results with the input voltage of 270 V, output voltage of 220 V rms and, with an output power of 2 kW. (a) Output voltage of inverter before filter, voltage of capacitor C_3, load voltage, and load current, (b) output voltage of inverter before filter, voltage of capacitor C_3, and voltage of capacitors C_1 and C_2, and (c) output voltage of inverter before filter, voltage of capacitor C_3, load voltage, and current of capacitor C_3.

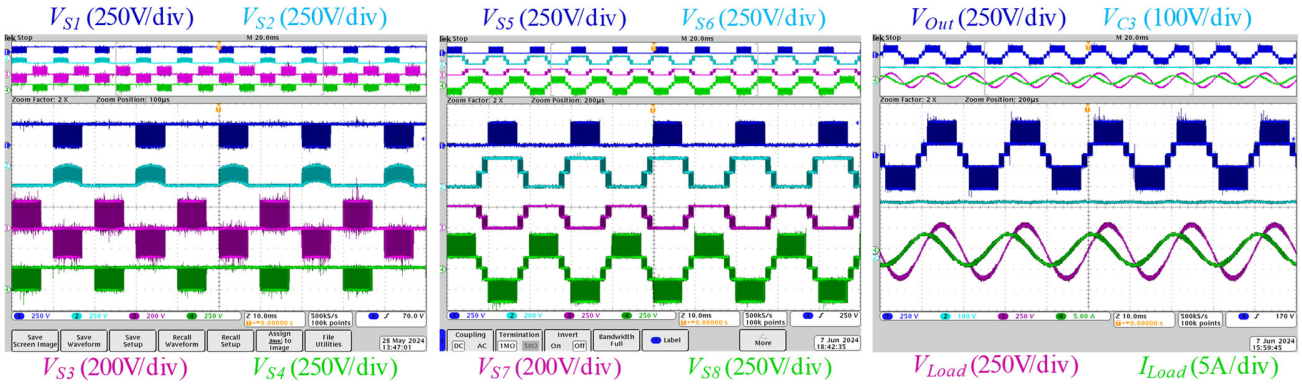

Fig. 7. (a) Voltage stress of switches S_1–S_4, (b) voltage stress of switches S_5–S_8, and (c) nonunity power factor load conditions: output voltage of inverter before filter, the voltage of capacitor C_3, load voltage, and load current with a phase difference of more than 80°.

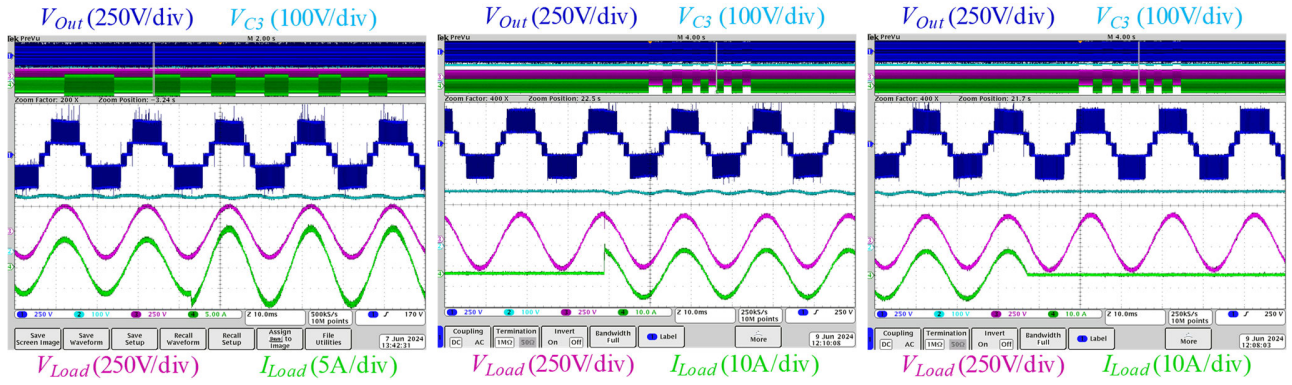

Fig. 8. Output voltage of the proposed inverter before the filter, voltage of capacitor C_3, load voltage, and load current during a step change in the output power. (a) Step change in the output power from 1.14 to 1.6 kW, (b) step change in the output power from 0 to 2 kW, and (c) load change from full power (2 kW) to 0.

2 kW, which has been measured as 97.43%. According to the values obtained for the efficiency, it can be concluded that the proposed inverter has a very high efficiency and can be used in renewable energy applications. The efficiency curve for various output powers, based on the mathematical calculations, is shown in Fig. 10. In Fig. 9, the experimental efficiency is measured using a power analyzer. These points are also plotted on the efficiency curve in Fig. 10.

The calculated efficiency values are very close to the measured values, demonstrating the accuracy of the loss and efficiency calculations. The loss breakdown of the proposed inverter is shown in Fig. 11, where the contribution of each component to the total losses is shown. To demonstrate the harmonic spectrum of the output voltage and current in the proposed inverter, a simulation was performed at an output power of 1 kW in grid-connected mode. Fig. 12 shows the

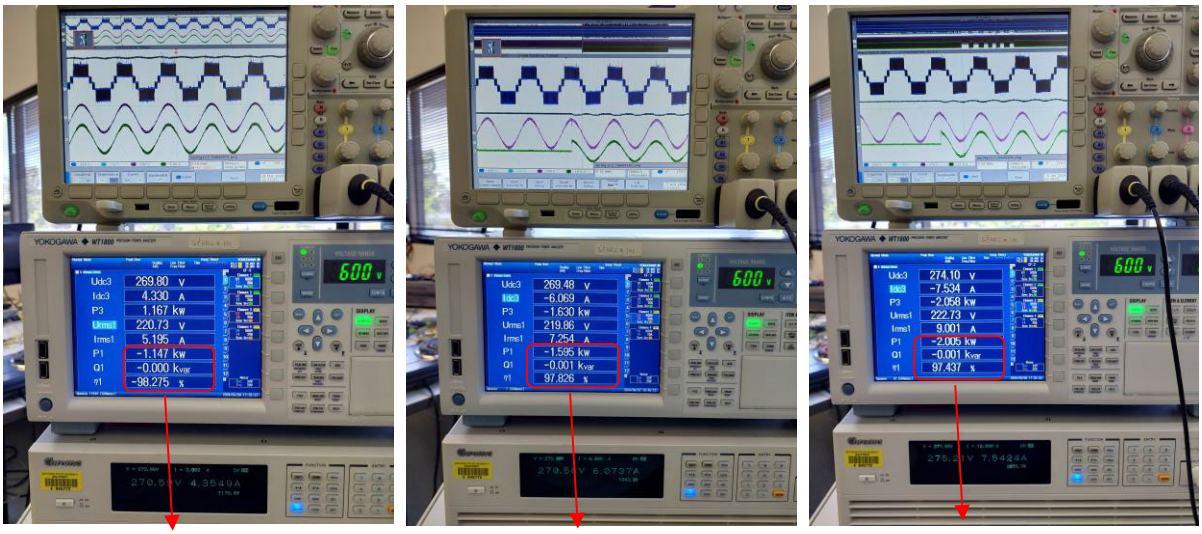

Fig. 9. Experimental efficiencies of the proposed inverter in different output powers and with an input voltage of 270 V. (a) 98.27% efficiency in the output power of 1.14 kW, (b) 97.82% efficiency in the output power of 1.59 kW, and (c) 97.43% efficiency in the output power of 2 kW.

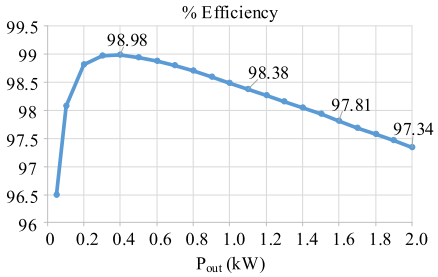

Fig. 10. Calculated efficiency of the proposed converter for different output power levels.

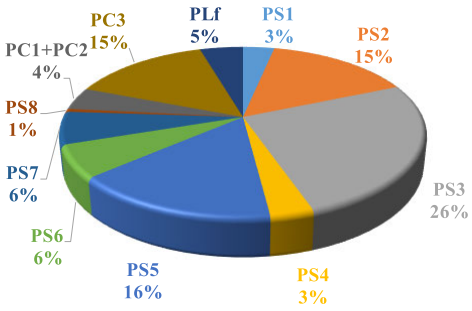

Fig. 11. Loss breakdown of the proposed inverter.

output voltage of the proposed inverter along with its harmonic spectrum. It can be observed from Fig. 12 that the rms value of the first harmonic is 311.1 V, and its THD is 47.84%. Additionally, Fig. 13 shows the current injected into the grid along with its harmonic spectrum. It can be seen that the THD of the injected current is 1.8%. According to IEEE Std 547-2018, which requires grid-connected inverters to have a current THD of less than 5%, the injected grid current of the proposed inverter meets this standard.

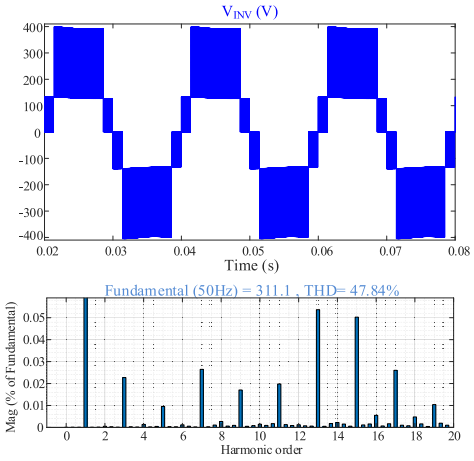

Fig. 12. Five-level output voltage of proposed inverter along with its harmonic spectrum and THD.

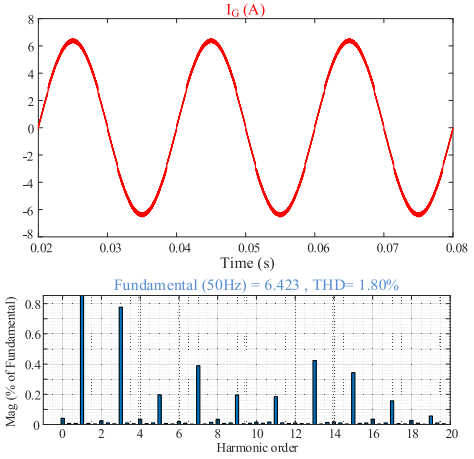

Fig. 13. Injected grid current in the proposed inverter along with its harmonic spectrum and THD.

VII. Conclusion

In this article, a novel five-level inverter based on NPC and a switched capacitor was proposed. The proposed inverter has the capability of voltage boosting with a gain of 1.5 and can transfer power from input to output in single-stage power processing. The ability to handle the reverse current made it possible to feed loads with a very low power factor. Also, the ability to reverse the current makes it possible to use the proposed inverter in battery storage systems. The single-stage power processing feature of the proposed inverter made it possible to achieve high efficiency. Despite the proposed inverter being multilevel, capacitor C_3 is charged and discharged at the switching frequency, which makes it possible to control the charging current range of this capacitor by controlling the switching frequency. Connecting the negative terminal of the output load to the midpoint of the input capacitors causes a constant common-mode voltage to be achieved. A complete comparison was made between the proposed inverter and other similar inverters to demonstrate the unique advantages of the proposed inverter. Finally, in order to prove the performance of the inverter, the experimental results with the output power of 2 kW were given.

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