A Novel Single-Phase Common Grounded Converter Based on Switched-Capacitor

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***Abstract*- This paper presents a new common grounded converter based on a switched capacitor (SC). The converter can be used as a suitable interface for single-phase AC or two-wire DC grids. The direct connection between the negative terminal of the input voltage source and the null terminal of the output source enables the elimination of the leakage current in renewable energy systems, especially in photovoltaic power generation. The proposed topology offers voltage-boosting capability, so there is no need for an additional boost converter and it is possible to inject power into the grid at DC input voltages lower than the peak value of the output voltage, which helps improve the efficiency of the converter. In addition, the proposed topology has the ability to handle reverse current, hence, it feeds non-unity power factor loads. The operating modes and design of passive components are described in detail. The performance and advantages of the proposed converter are compared with other converters. Finally, through the experiment on a (3.78 kW/7 kW) converter, the performance of the proposed converter is validated.**

***Index Terms*—Common grounded converter, voltage boosting, single-stage system.**

I. Introduction

The ever-increasing energy demands of humanity have led to a pressing need for new energy sources. It is estimated that by 2050, the global consumption of electrical energy will have been doubled, which highlights the urgency of sustainable energy options like solar and wind power, as well as other Renewable Energy Sources (RESs), to meet this demand. However, given the scale of this task, it is evident that the current electric infrastructure will not be sufficient to support the transition. To mitigate this challenge, storage elements will be essential in balancing the grid with a high level of RES penetration. Presently, there is no viable business model for this purpose. Additionally, the issue of storage battery utilization looms as a potential obstacle.

The resurgence of interest in DC microgrids is largely due to the fact that most RESs and battery storages are DC-based [1]-[2]. This trend is gaining momentum and has become a modern-day phenomenon [3]-[6]. A preferred DC voltage level of 325 V has been identified as the most technically and economically viable option [5]. However, some studies suggest that a DC voltage level ranging from 350 to 380 V could become the future standard [7]. To implement this, a 3-wire DC grid configuration is being considered, comprising +350 V, -350 V, and a neutral point. Despite the potential advantages of such a grid, certain problems have been identified. Alternatively, a 700 V DC grid has been proposed as an islanding microgrid for RES integration. While this grid would allow for efficient energy transfer, it would not be compatible with most household devices. In conclusion, the swift implementation of DC solutions is hindered by the rapidly evolving power electronics landscape and market uncertainty. This presents a major challenge for large market players looking to invest in these technologies. Despite the clear advantages of DC grids, the absence of a viable business model has been identified as the primary obstacle to their widespread adoption. As a result, investors are hesitant to fund DC projects, and power electronics manufacturers are not rushing to produce DC-compatible appliances. One potential solution to this problem could be the development of power electronics converters that can be used for both DC and AC applications [8], [9]. This approach would help mitigate the risks associated with investing in the DC infrastructure, while also providing greater flexibility for consumers. This concept is shown in Fig. 1.

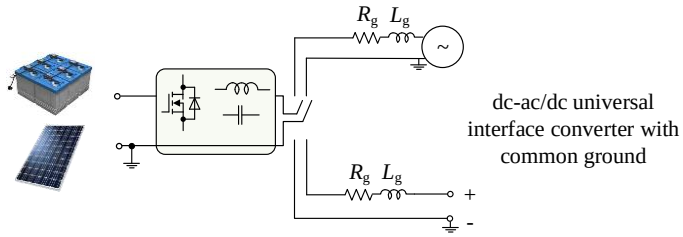


Fig. 1. Universal DC-DC/AC interface converter concept.

In parallel, several technical considerations need to be addressed when implementing dc grids. Of these, grounding and protection issues are of utmost importance [10]. Numerous approaches to grounding design in electric power systems have been proposed, each with a unique set of benefits and drawbacks that affect the overall system performance [11]. Grounding is primarily used for ground fault detection [12], as well as for the safety of personnel and equipment. In the case of low voltage (LV) DC microgrids, grounding can be achieved through either high or low-resistance grounding, with the ground connected to one of the poles or the middle point, depending on availability. In the context of grounding, low resistance grounding refers to a grounded wire that has a potential very similar to that of an AC grid. However, when designing the grounding of a DC installation, it is important to consider the potential for corrosion of the materials involved. This is because DC leakage currents can cause electrochemical reactions that may be harmful to concrete structures. To mitigate this issue, anti-parallel diodes can be used in series with the ground. The use of such diodes is recommended in the NPR 9090:2018 standard as a method of preventing corrosion-related damage to the installation.

The grounding approach utilized in DC grid systems is also influenced by the nature of the interconnection between the AC and DC grids. In situations where power is transferred between the AC and DC microgrids, this can be achieved through the use of a low-frequency transformer in combination with a non-isolated front-end rectifier. In the case of non-isolated power electronics

interfaces, DC-AC energy conversion with a common ground is typically the most effective solution.

Several DC-AC converters with common ground capability are presented in [13]-[17]. These converters are based on flying inductors (FI), which have the ability to increase the input voltage and can inject power to the output at input DC voltages lower than the peak voltage of the grid. However, since these converters are based on the charging and discharging of the inductor, a large inductor is needed. In [18], a common grounded converter based on a flying capacitor (FC) is presented. Due to the presence of the boost converter at the input of this topology, it is possible to operate at input voltages lower than the peak value of the output voltage. In this converter, the combination of an inductor and a capacitor is used to transfer power from the input source to the output, which makes the volume of the inductor used in the converter high. In [19]-[21], several three-level common grounded converters based on a switched capacitor (SC) are presented. In these topologies, a capacitor is used to pump power from the input source to the output grid. Since these typologies lack the capability of voltage boosting, they need a boost converter for their input so that the power transmission process can be performed at lower input voltages than the peak voltage of the grid. The presence of an additional boost converter affects the efficiency and volume of the entire system. In [22]-[25], several three-level and five-level common grounded converters based on SC are presented. Although these converters have voltage boosting capability, their voltage gain is limited to two and they will need an additional boost converter at a lower input voltage. Also, two six-level and seven-level typologies are proposed in [26] and [27], respectively, which are a combination of a SC and a neutral point clamp (NPC) converter. Although the leakage current in these topologies is not completely eliminated, its value is low. In addition, their voltage gain is limited to 1.5 and they will need an additional boost converter at a lower input voltage.

The main purpose of this paper is to present a superior solution that can work in the DC-AC and the DC-DC mode at the same output terminal. The proposed new SC structure with a common ground feature has the capability of four times voltage boosting and can perform the power transfer process from the input source to the output in a wide range of input voltage. The ability to have a common ground eliminates leakage current in the system, and the ability to handle return current provides the possibility of feeding non-unity power factor loads.

In the following, Section II explains the structure of the proposed converter. The operation modes of the SC-based converter in the DC-AC condition are outlined in Section III. The switching duty cycle of the inverter is computed in Section IV. Design considerations for all key components of the solution are described in Section V. The Control system strategy of the proposed converter is explained in Section VI. Section VII focuses on the comparative evaluation to validate the performance and feasibility of the SC converter, while Section VIII provides some experimental results. In the concluding section, the feasibility of the proposed converter is discussed.

II. The Proposed Nine-Level Common Grounded Converter

The topology of the proposed 9-level inverter is shown in Fig. 2(a). In this inverter, nine power electronic switches, two power diodes, and three capacitors are used to produce a nine-level output voltage. Eight of the switches used in this inverter are unidirectional and only one switch is bi-directional. For unidirectional switches, a normal MOSFET with an internal antiparallel diode can be used. For the bidirectional switches of the proposed inverter, it is possible to use the series connection of a MOSFET and a diode or the back-to-back series connection of two MOSFETs, as shown in Fig. 2(b). It should be noted that the losses of two series MOSFETs with back-to-back connections are lower than in the series connection of a MOSFET and a diode. In addition, in order to increase the efficiency of the inverter, active diodes can be used instead of ordinary diodes. According to Fig. 2(a), there is a direct connection between the negative terminal of the input voltage source and the neutral terminal of the output power grid. This feature is suitable for power electronic interfaces used in renewable energy systems, especially photovoltaic systems. As a result, the leakage current caused by parasitic capacitors in photovoltaic systems is eliminated. Furthermore, the ability to handle reverse current in the proposed inverter makes it possible to control the reactive power at the point of common coupling (PCC) and in the grid-following mode. This inverter enables feeding non-unity power factor loads in the grid-forming mode. Considering that the proposed converter is common-ground and can produce DC voltage with positive and negative polarity in its output terminal, this converter can be used as a suitable interface for AC or DC output application.

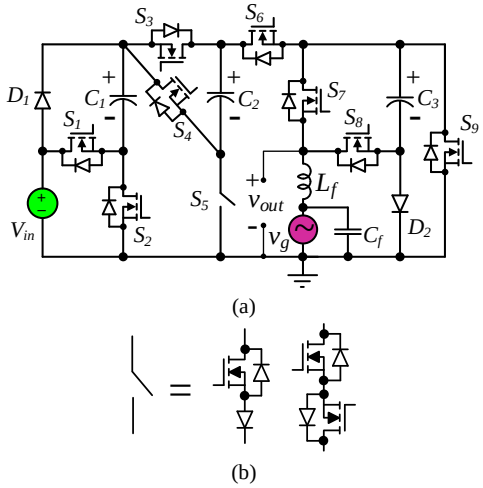


Fig. 2. (a) The proposed nine-level SC-based common-grounded inverter, (b) bidirectional switches used in the inverter.

The proposed inverter has the ability to boost the voltage up to four times the input voltage. Therefore, in the grid-forming and the grid-following mode and at an input voltage lower than the peak value of the output voltage, it can feed the load or the grid. In this inverter, the capacitor C_1 is charged as much as the input voltage, the capacitor C_2 is charged to twice the input voltage, and the capacitor C_3 is charged to four times the input voltage. Since the proposed inverter is based on the SC technology, the capacitors

are self-balancing, and no additional controller is needed to control the voltage of the capacitors.

III. Operation Modes of the Proposed Topology in DC-AC State

Fig. 3 shows the operating modes of the proposed inverter. The inverter has nine operation modes, of which four operation modes are related to the positive half-cycle and another four to the negative half-cycle. Another operation mode is related to the zero-voltage vector, which is the same for positive and negative half-cycles. In the operation modes, the active power path is shown with red lines, the reactive power path with green lines, and the capacitor charging path with blue lines. Next, the working modes of the proposed inverter will be discussed.

A. Zero-level operation mode

The equivalent circuit of the proposed inverter at zero level is shown in Fig. 3(a). In this operation mode, switches S_1, S_4, S_6, S_8 and the diode D_2 are on, which causes zero voltage to be produced at the output of the inverter. In order to produce zero voltage at the output of the inverter, the series connection of the input voltage source with capacitors C_1, C_2, and C_3 is used. Since the polarity of the capacitor C_3 is connected inversely with the polarity of capacitors C_1 and C_2 and the input voltage source, the output voltage is zero in this operation mode. This mode is the same for the positive and the negative half-cycle. In this operating mode, capacitors C_1 and C_2 are in the discharging state and capacitor C_3 is in the charging state.

$$v_{out} = V_{in} + V_{C_1} + V_{C_2} - V_{C_3} = 0 \tag{1}$$

B. First-level operation mode in the positive half-cycle

The equivalent circuit of the proposed inverter in the first-level operation mode of the positive half-cycle is shown in Fig. 3(b). In this mode, when switches S_3, S_6, S_7, and the diode D_1 are turned on, $+V_{in}$ voltage is produced at the output of the inverter. In other words, the output voltage of the inverter is equal to the input voltage. Turning on switch S_2 in this way causes the capacitor C_1 to be charged by the input source and through the diode D_1. In this operation mode, capacitors C_2 and C_3 are also in a disconnecting state.

$$v_{out} = V_{in} \tag{2}$$

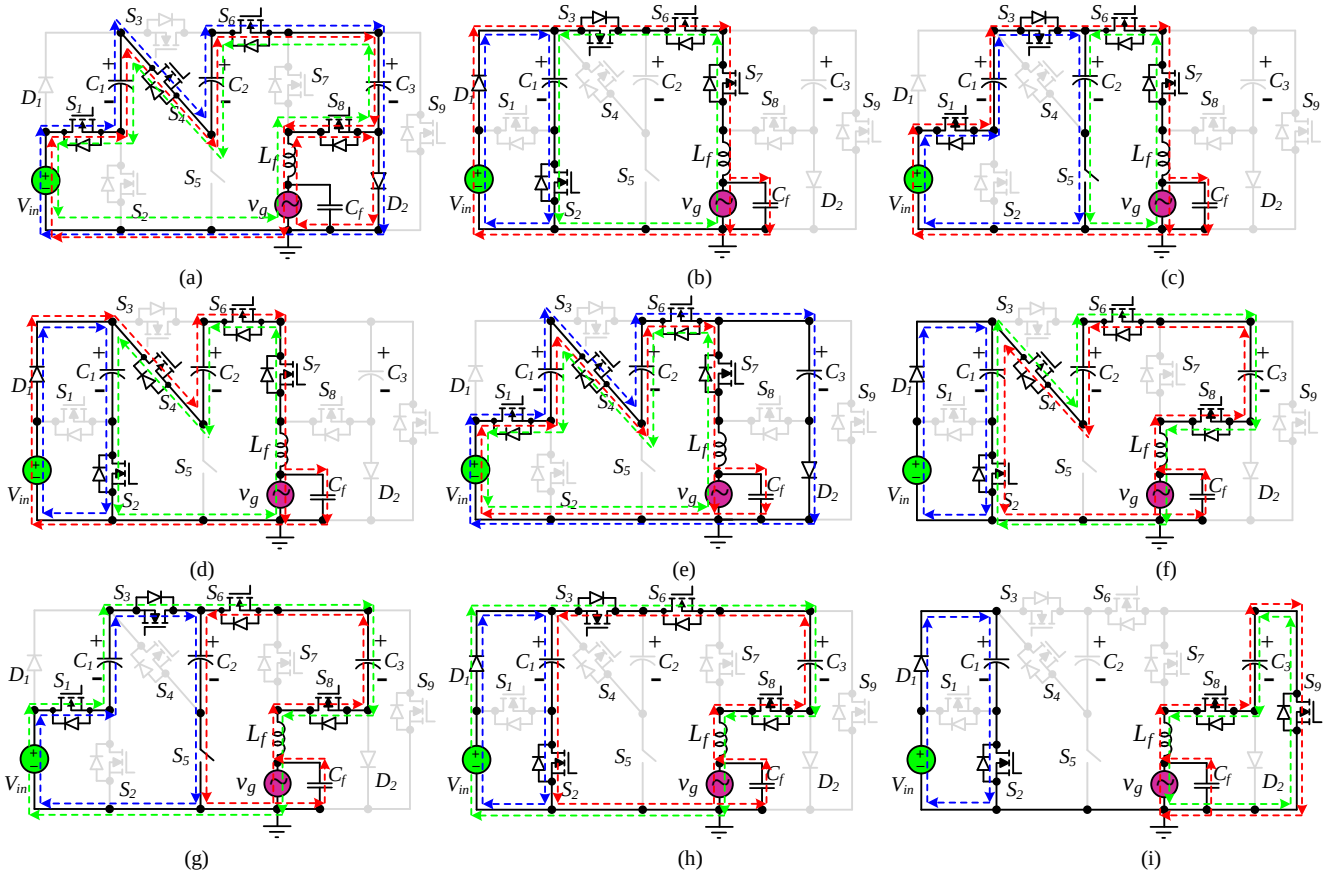


Fig. 3. Operation modes of the proposed 9-level inverter: (a) zero level, 0; (b) first level in the positive half-cycle, $+V_{in}$; (c) second level in the positive halfcycle, $+2V_{in}$; (d) third level in the positive half-cycle, $+3V_{in}$; (e) fourth level in the positive half-cycle, $+4V_{in}$; (f) first level in the negative half-cycle, $-V_{in}$; (g) second level in the negative half-cycle, $-2V_{in}$; (h) third level in the negative half-cycle, $-3V_{in}$; (i) fourth level in the negative half-cycle, $-4V_{in}$.

C. Second-level operation mode in the positive half-cycle

The equivalent circuit of the proposed inverter in the second level operation mode of the positive half-cycle is shown in Fig. 3(c). Switches S_1, S_3, S_6, and S_7 are on in this operation mode and cause the series connection of the input voltage source with the capacitor C_1 to produce $+2V_{in}$ voltage at the output of the inverter. When the switch S_5 is turned on, the capacitor C_2 will be charged twice as much as the input voltage. In this operating mode, the capacitor C_1 is in the discharging and the capacitor C_3 is in the disconnecting state.

$$v_{out} = V_{in} + V_{C_1} = +2V_{in} \tag{3}$$

D. Third-level operation mode in the positive half-cycle

The equivalent circuit of the proposed inverter in the third-level operation mode of the positive half-cycle is shown in Fig.3 (d). Turning on switches S_4, S_6, and S_7 along with the diode D_1 causes the voltage of the input source to be transferred to the output of the inverter along with the voltage of the capacitor C_2; thus, the output voltage of the inverter is equal to $+3V_{in}$. Turning on the switch S_2 causes the capacitor C_1 to be charged by the input source and through the diode D_1. In this operation mode, the capacitor C_2 is in the discharging state and the capacitor C_3 is in the disconnecting state.

$$v_{out} = V_{in} + V_{C_2} = +3V_{in} \tag{4}$$

E. Fourth-level operation mode in the positive half-cycle

In order to produce the fourth voltage level at the output of the proposed inverter, capacitors C_1 and C_2 need to be connected in series with the input voltage source. In order to generate $+4V_{in}$ voltage at the output of the inverter, it is necessary to turn on switches S_1, S_4, S_6, and S_7. Turning on the diode D_2 causes the capacitor C_3 to be charged four times the input voltage. Therefore, in this operating mode, capacitors C_1 and C_2 are in the discharging mode and capacitor C_3 is in the charging mode. The equivalent circuit of the fourth-level operation mode in the positive half-cycle is shown in Fig. 3(e).

$$v_{out} = V_{in} + V_{C_1} + V_{C_2} = +4V_{in} \tag{5}$$

F. First-level operation mode in the negative half-cycle

The equivalent circuit of the proposed inverter in the first-level operation mode of the negative half-cycle is shown in Fig. 3(f). In this operating mode, switches S_2, S_4, S_6 and S_8 are on and cause the generated voltage by the series connection of three capacitors C_1, C_2 and C_3 to be transferred to the output of the inverter. The output voltage in this operating mode is equal to $-V_{in}$. The duty of the supplying power in the negative half-cycle is the responsibility of the capacitor C_3. Turning on the diode D_1 also causes the capacitor C_1 to be charged from the input source. In summary, capacitors C_1 and C_2 are charged in this operating mode, and the capacitor C_3 is discharged.

$$v_{out} = V_{C_1} + V_{C_2} - V_{C_3} = -V_{in} \tag{6}$$

G. Second-level operation mode in the negative half-cycle

In order to be able to produce $-2V_{in}$ voltage at the output of the inverter, it is necessary to transfer the voltage caused by connecting capacitors C_2 and C_3 in series to the output of the inverter. For this purpose, switches S_5, S_6, and S_8 need to be turned on. Turning on switches S_1, S_3 causes the capacitor C_1 to charge the capacitor C_2 along with the input voltage source. Thus, in this operating mode, capacitors C_1 and C_3 are discharged and the capacitor C_2 is charged. The equivalent circuit of the proposed inverter in this operation mode is shown in Fig. 3(g). The output voltage of the inverter in this working mode is equal to $-2V_{in}$.

$$v_{out} = V_{C_2} - V_{C_3} = -2V_{in} \tag{7}$$

H. Third-level operation mode in the negative half-cycle

Fig. 3(h) shows the equivalent circuit of the proposed inverter in the third-level operation mode of the negative half-cycle. In order to produce $-3V_{in}$ voltage at the output of the inverter, it is necessary to transfer the voltage resulting from the series connection of capacitors C_3 and C_1 to the output of the inverter. For this purpose, switches S_2, S_3, S_6 and S_8 are turned on. Diode D_1 is also active in this working mode so that it can charge the capacitor C_1 from the input source if needed. In general, in this working mode, the capacitor C_3 is discharged, the capacitor C_1 is charged and the capacitor C_2 is in the disconnecting mode.

$$v_{out} = V_{C_1} - V_{C_3} = -3V_{in} \tag{8}$$

I. Fourth-level operation mode in the negative half-cycle

Finally, in order to produce $-4V_{in}$ voltage at the output of the proposed inverter, the voltage of the capacitor C_3 is connected to the output of the inverter alone, which causes $-4V_{in}$ voltage to be produced. For this purpose, switches S_8 and S_9 need to be turned on, and the switch S_2 is turned on along with the diode D_1, which causes the capacitor C_1 to be charged from the input source. In general, in this operating mode, the capacitor C_1 is charged, the capacitor C_3 is discharged, and the capacitor C_2 is disconnected. The equivalent circuit of the proposed inverter in the fourth-level operation mode of the negative half-cycle is shown in Fig. 3(i).

$$v_{out} = -V_{C_3} = -4V_{in} \tag{9}$$

In order to better understand the operating modes of the proposed topology, Table I shows the status of the switched-on switches as well as the charging and discharging status of the capacitors in different modes. The "↑" sign means charging the capacitor, the "↓" sign means discharging the capacitor, and the "–" sign means disconnecting the capacitor.

TABLE I.
SWITCHING STATE OF THE PROPOSED NINE-LEVEL INVERTER.

Levels	Involved switches	Capacitor's Mode			Output voltage
		C_1	C_2	C_3	
1st (P)	S_2, S_3, S_6, S_7	↑	-	-	$+V_{in}$
2nd (P)	S_1, S_3, S_5, S_6, S_7	↓	↑	-	$+2V_{in}$
3rd (P)	S_2, S_4, S_6, S_7	↑	↓	-	$+3V_{in}$
4th (P)	S_1, S_4, S_6, S_7	↓	↓	↑	$+4V_{in}$
Zero	S_1, S_4, S_6, S_8	↓	↓	↑	0
1st (N)	S_2, S_4, S_6, S_8	↑	↑	↓	$-V_{in}$
2nd (N)	S_1, S_3, S_5, S_6, S_8	↓	↑	↓	$-2V_{in}$
3rd (N)	S_2, S_3, S_6, S_8	↑	-	↓	$-3V_{in}$
4th (N)	S_2, S_8, S_9	↑	-	↓	$-4V_{in}$

IV. SWITCHING DUTY CYCLE CALCULATION FOR THE PROPOSED NINE-LEVEL INVERTER

The 9-level output voltage of the proposed inverter along with the grid voltage in the positive half-cycle and negative half-cycle is shown in Fig. 4. According to this figure, the output voltage of the inverter in the positive half-cycle can be defined in Zone1, Zone2, Zone3, and Zone4. Each of the zones has a different switching duty cycle, which will be calculated in the following. The grid voltage and the grid current in the unity power factor are expressed by (10) and (11):

$$v_g(t) = V_{\max} \sin \omega t \tag{10}$$

$$i_g(t) = I_{\max} \sin \omega t \tag{11}$$

A. Zone1

According to Fig. 4, in Zone1, the output voltage of the inverter changes between zero and V_{in}. By applying the voltage balance law on the output inductor L_f in a complete switching cycle, the duty cycle of the inverter in Zone1 is obtained as follows:

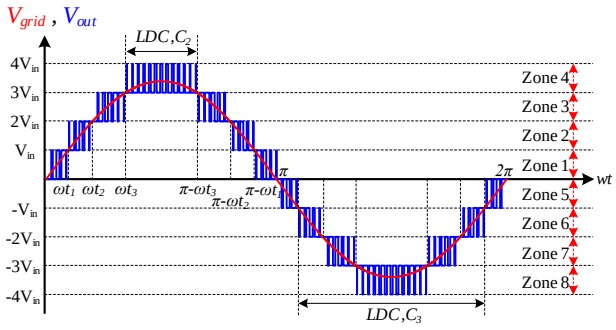


Fig. 4. Nine-level output voltage of the inverter and grid voltage.

$$\int_0^{d_1T_s}(V_{in}-v_g)dt+\int_{d_1T_s}^{T_s}(-v_g)dt=0 \tag{12}$$

$$d_1(t)=\frac{v_g(t)}{V_{in}}=\frac{V_{\max}}{V_{in}}\cdot\sin\omega t \quad ; \quad 0\le t<t_1 \tag{13}$$

In (12), T_s is the switching period of the inverter.

B. Zone2

It is clear from Fig. 4 that the output voltage of the inverter in Zone2 changes between V_{in} and $2V_{in}$. By applying the voltage balance law on the output inductor L_f in a complete switching cycle, the duty cycle of the inverter in Zone2 is obtained as follows:

$$\int_0^{d_2T_s}(2V_{in}-v_g)dt+\int_{d_2T_s}^{T_s}(V_{in}-v_g)dt=0 \tag{14}$$

$$d_2(t)=\frac{v_g(t)}{V_{in}}-1=\frac{V_{\max}}{V_{in}}\cdot\sin\omega t-1 \quad ; \quad t_1\le t<t_2 \tag{15}$$

C. Zone3

Fig. 4 shows that the output voltage of the inverter in Zone3 changes between $+2V_{in}$ and $+3V_{in}$, so by applying the voltage balance law on the output inductor L_f in a complete switching cycle, the duty cycle of the inverter in Zone3 is calculated as follows:

$$\int_0^{d_3T_s}(3V_{in}-v_g)dt+\int_{d_3T_s}^{T_s}(2V_{in}-v_g)dt=0 \tag{16}$$

$$d_3(t)=\frac{v_g(t)}{V_{in}}-2=\frac{V_{\max}}{V_{in}}\cdot\sin\omega t-2 \quad ; \quad t_2\le t<t_3 \tag{17}$$

D. Zone4

From Fig. 4, it is clear that the output voltage of the inverter in Zone4 changes between $+3V_{in}$ and $+4V_{in}$. Therefore, to calculate the duty cycle, it is necessary to write the voltage balance law in a complete switching cycle for the output inductor L_f. Equations (18) and (19) show how to calculate the duty cycle for Zone4.

$$\int_0^{d_4T_s}(4V_{in}-v_g)dt+\int_{d_4T_s}^{T_s}(3V_{in}-v_g)dt=0 \tag{18}$$

$$d_4(t)=\frac{v_g(t)}{V_{in}}-3=\frac{V_{\max}}{V_{in}}\cdot\sin\omega t-3 \quad ; \quad t_3\le t<\frac{T}{2}-t_3 \tag{19}$$

In order to calculate the time values t_1, t_2, and t_3, equations (20)-(22) are used.

$$t_1=\frac{1}{\omega}\sin^{-1}\left(\frac{V_{in}}{V_{\max}}\right) \tag{20}$$

$$t_2=\frac{1}{\omega}\sin^{-1}\left(\frac{2V_{in}}{V_{\max}}\right) \tag{21}$$

$$t_3=\frac{1}{\omega}\sin^{-1}\left(\frac{3V_{in}}{V_{\max}}\right) \tag{22}$$

Using the symmetry of the circuit operation, the negative half-cycle switching patterns can be easily derived. It is omitted here for simplicity. The duty cycle of each of the switches in different operating Zones is shown in Table II.

TABLE II
THE DUTY CYCLE OF SWITCHES IN DIFFERENT OPERATING ZONES.

	Switches	S1	S2	S3	S4	S5	S6	S7	S8	S9
Positive half-cycle	**Zone 1**	1-$d_1(t)$	$d_1(t)$	$d_1(t)$	1-$d_1(t)$	0	1	$d_1(t)$	1-$d_1(t)$	0
	Zone 2	$d_2(t)$	1-$d_2(t)$	1	0	$d_2(t)$	1	1	0	0
	Zone 3	1-$d_3(t)$	$d_3(t)$	1-$d_3(t)$	$d_3(t)$	1-$d_3(t)$	1	1	0	0
	Zone 4	$d_4(t)$	1-$d_4(t)$	0	1	0	1	1	0	0
Negative half-cycle	**Zone 5**	1-$d_1(t)$	$d_1(t)$	0	1	0	1	0	1	0
	Zone 6	$d_2(t)$	1-$d_2(t)$	$d_2(t)$	1-$d_2(t)$	$d_2(t)$	1	0	1	0
	Zone 7	1-$d_3(t)$	$d_3(t)$	1	0	1-$d_3(t)$	1	0	1	0
	Zone 8	0	1	1-$d_4(t)$	0	0	1-$d_4(t)$	0	1	$d_4(t)$

V. CALCULATION OF THE OUTPUT FILTER INDUCTOR AND CAPACITORS

In this section, the value of the output filter inductor along with the value of the filter capacitors C_1, C_2 and C_3 are calculated.

A. Calculation of the output filter inductor

In order to calculate the value of the output filter inductor, the inductor current equation can be written in each of the zones of the inverter. Since the current ripple of L_f has its highest value in Zone4, the current equation for i_L(t) is written in Zone4.

$$i_{Lf}(t)=\frac{1}{L_f}\int_0^t V_{Lf}\,dt+i_{Lf}(0) \quad ; \quad t_3\le t<\frac{T}{2}-t_3 \tag{23}$$

By simplifying (23) and inserting (19) into it, the inductor value of the output filter is obtained as follows:

$$L_f=\frac{1}{\Delta I_{L_f}\cdot f_s}\left(7V_{\max}\sin(\omega t)-\frac{V_{\max}^2}{V_{in}}\cdot\sin^2(\omega t)-12V_{in}\right) \tag{24}$$

At the unity power factor, the maximum current ripple of the inductor L_f occurs at ωt=π/2. Therefore, the value of L_f for the maximum current ripple is calculated as follows:

$$L_f=\frac{1}{\Delta I_{L_f,\max}\cdot f_s}\left(7V_{\max}-\frac{V_{\max}^2}{V_{in}}-12V_{in}\right) \tag{25}$$

To calculate the value of the output filter capacitor C_f, the capacitor voltage equation can be written for each of the operating zones. Since the maximum voltage ripple of the output filter capacitor occurs in Zone4, the capacitor voltage equation C_f for this zone is written:

$$v_{Cf}(t)=\frac{1}{C_f}\int_0^t i_{Cf}\,dt+v_{Cf}(0)\quad;\quad t_3\le t<\frac{T}{2}-t_3 \tag{26}$$

$$\Delta V_{Cf}=\frac{\Delta I_{Lf}}{8C_f f_s}\quad;\quad t_3\le t<\frac{T}{2}-t_3 \tag{27}$$

$$C_f=\frac{1}{8\Delta V_{Cf}\cdot L_f\cdot f_s^{\,2}}\left(7V_{g,\max}\sin(\omega t)-\frac{V_{g,\max}^2}{V_{in}}\cdot\sin^2(\omega t)-12V_{in}\right) \tag{28}$$

By placing (24) in (27) and simplifying it, equation (28) can be obtained. At the unity power factor, the maximum voltage ripple of the output filter capacitor occurs at ωt=π/2. Therefore, the value of C_f for the maximum voltage ripple is calculated as follows:

$$C_f=\frac{1}{8\Delta V_{Cf,\max}\cdot L_f\cdot f_s^{\,2}}\left(7V_{g,\max}-\frac{V_{g,\max}^2}{V_{in}}-12V_{in}\right) \tag{29}$$

B. Calculation of capacitors C_1, C_2 and C_3

The value of capacitors C_1, C_2, and C_3 will be different in the multi-level and the three-level operating mode. In the multi-level operating mode, since the charging and discharging currents of capacitors C_1, C_2, and C_3 have a fraction of the fundamental frequency, more capacitance is needed to have the allowable voltage ripple value in the capacitors. In the three-level operating mode, since the charging and discharging current of the capacitors works at the switching frequency, a high capacitance is not needed to achieve the allowable voltage ripple value in the capacitors. To calculate the value of the capacitors in the multi-level mode, the longest discharge (LDC) time can be used, which is shown in Fig. 4. Therefore, the capacitance values of capacitors C_1, C_2 and C_3 are calculated by the following relations:

$$C_1=\frac{2P_{out}\left(V_{\max}-3V_{in}\right)}{\Delta V_{C1,\max}\cdot f_s\cdot V_{in}\cdot V_{\max}} \tag{30}$$

$$C_2=\frac{\int_{\omega t_3}^{\pi-\omega t_3} i_{C2}\,d(\omega t)}{\Delta V_{C2,\max}}=\frac{4P_{out}\cdot\cos\left(\sin^{-1}\left(\frac{3V_{in}}{V_{\max}}\right)\right)}{\Delta V_{C2,\max}\cdot V_{\max}} \tag{31}$$

$$C_3=\frac{\int_{\pi+\omega t_1}^{2\pi-\omega t_1} i_{C3}\,d(\omega t)}{\Delta V_{C3,\max}}=\frac{4P_{out}\cdot\cos\left(\sin^{-1}\left(\frac{V_{in}}{V_{\max}}\right)\right)}{\Delta V_{C3,\max}\cdot V_{\max}} \tag{32}$$

In (30), (31) and (32), the parameters $\Delta V_{C1,\max}$, $\Delta V_{C2,\max}$, $\Delta V_{C3,\max}$, and P_{out} are the voltage ripple of capacitors C_1, C_2, C_3, and the injected power to the grid, respectively. The value of the capacitors in the three-level operating mode is calculated as follows:

$$C_1=C_2=C_3=\frac{2P_{out}}{3V_{in}\cdot\Delta V_{C,\max}\cdot f_s} \tag{33}$$

Double-line frequency power ripple is one of the characteristics of single-phase systems. If the input voltage source is a battery or a constant voltage source, then there is no need to remove this power ripple from the input source, but if the input voltage source is a PV, then the power ripple should be removed from the input source. For this purpose, two active and passive methods are used. In the passive method, a parallel capacitor is used with the input voltage source, which is calculated by the following equation:

$$C_{in}=\frac{P_{in}}{2\pi\cdot f_{grid}\cdot V_{dc}\cdot\Delta V_{C,in}}=\frac{P_{out}}{2\pi\cdot f_{grid}\cdot V_{dc}\cdot\Delta V_{C,in}\cdot\eta} \tag{34}$$

An advantage of switch-capacitor converters is that they require no additional controller to balance the voltage of the capacitors. However, the disadvantage of these converters is the spike charging current of the capacitors. The spike charging current increases the current stress of the switches. It is possible to reduce the voltage ripple of the capacitors by choosing the right value of the capacitors and thereby reduce the spike of the capacitor charging current and the current stress of the switches. It is also possible to reduce the level of EMI in the converter by proper PCB design for the power board. However, this issue was addressed during PCB design where all switching cells were carefully designed.

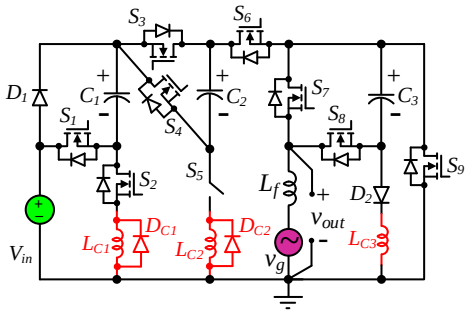


Fig. 5. Proposed converter with capacitive charging current spike limiting strategy.

As a result, spreading of the electromagnetic field was minimized. In fact, it is one of the reasons of our good results related to good efficiency. Another way to reduce the spike charging current in SC converters is to use a low value inductor in the charging path of the capacitors. The location of these inductors in the proposed converter is shown in Fig. 5. This technique is described in [36]. In Fig. 5, the charging current of each of the capacitors C_1, C_2 and C_3 passes through the inductors L_{C1}, L_{C2} and L_{C3}, and thus, the spike charging current of the capacitors is limited. Considering that the inductors L_{C1} and L_{C2} are placed in series with the switches S_2 and S_5, to ensure that there is a current path for these inductors when the switches S_2 and S_5 are turned off, the diodes D_{C1} and D_{C2} are paralleled with the inductors L_{C1} and L_{C2}. But a parallel diode is not necessary for the inductor L_{C3} because this inductor is in series with the diode D_2 and can form its path through the capacitor C_3 and the internal diode of the switch S_9.

It is important to mention that the experimental results in this study were obtained without the presence of inductors L_{C1}, L_{C2} and L_{C3} and diodes D_{C1} and D_{C2}. Appropriate and accurate design of

the power board has made it possible to obtain experimental results from the proposed converter in the DC-DC mode up to 7 kW and in the DC-AC mode up to 3.78 kW, without EMI being able to disrupt the operation of the microcontroller and its reset. Also, the proposed converter showed high efficiency, which was directly measured by the power analyzer.

VI. Control System Description

Fig. 6 illustrates the block diagram of the control strategy for the proposed converter. The study considers various control modes. Prior to connecting the grid-side slid-state circuit breaker (SSCB), the control system identifies the type of the grid available. In the case of an ac grid, the phase-locked loop (PLL) ensures synchronization. Once the voltage zero crossing is detected, the SSCB is connected to the grid, and the AC grid-connected algorithm becomes operational. If the PLL fails to detect the AC grid, the control system checks the DC voltage.

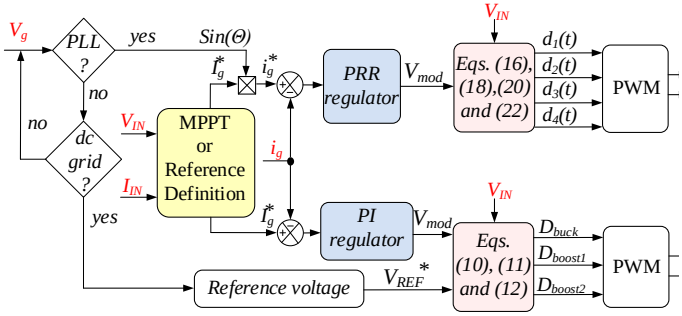


Fig. 6. Simplified block diagram of the applied control system.

If the DC grid is detected, the output capacitor is pre-charged to the same voltage level, and SSCB switches on with the appropriate DC current control mode. The control system can employ various methods for the grid current controller, whether for DC or AC grids. No additional computational resources are needed, as only one strategy (DC or AC) is used at any given time. The control system is capable of injecting DC and AC harmonics, which are utilized to detect islanding operation. When islanding is detected, the converter halts and restarts only after receiving the corresponding external permission for the grid-forming operation. For solar applications, the maximum power point tracking (MPPT) block is essential to adjust the reference grid current (I_g*) based on the observed operation point on the PV array. The approach for solar converters is similar. In battery applications, the MPPT block is replaced by reference current generation, considering measured voltage (V_{in}) and current (I_{in}). In the case of AC grid connection, the AC reference grid current (i_g*) is derived by multiplying the reference current (I_g*) with a sinusoidal signal from the PLL block. The reference i_g* waveform is synchronized with the fundamental component from the voltage at the point of common coupling (PCC) (V_g) using scalable factors. The difference between the reference i_g* and the real grid current (i_g) is then provided to the current control block. The current controller produces a reference voltage (V_{MOD}*) to be applied across the output capacitor (C_f). The intermediate calculation block utilizes the measured input voltage to determine the corresponding duty cycles required for realizing this voltage. These values are then fed to the pulse width modulation (PWM) block. The MPPT and PLL blocks are not discussed in detail here. It can be concluded from the literature review that a conventional second order generalized integrator (SOGI) regulator is one the best options for PLL [31]. Similarly, the most common methods for the realization of MPPT are the perturb and observe (P&O) or incremental conductance (IC). Some of the studies utilize modifications of the P&O or IC MPPT methods [32]-[35]. Various options exist for implementing the grid current control. In this case, the proportional-resonant and repetitive (PRR) controller is used for the AC mode, while the PI controller is employed for the DC mode. Detailed tuning of the PRR controller is described in [28], [29], and [30]. A proportional component eliminates possible injection of the DC current into the grid. Additionally, alternative nonlinear methods like Model Predictive Control (MPC) could be considered, as they have been found to be feasible for industrial implementation and suitable for achieving desired output currents in the discussed solutions.

In common-grounded converters, due to the direct connection of the negative terminal of the input DC source and the neutral terminal of the AC grid, in the positive half-cycle, the injected power to the output or AC grid is supplied directly from the input source. But in the negative half-cycle, the injected power to the output or AC grid is supplied by the energy stored in the capacitor or the inductor (in this proposed converter, it is provided by the capacitor). Therefore, it can have some DC-offset in the output current, which is not a problem specific to the converter proposed here, and all common-grounded converters have this problem.

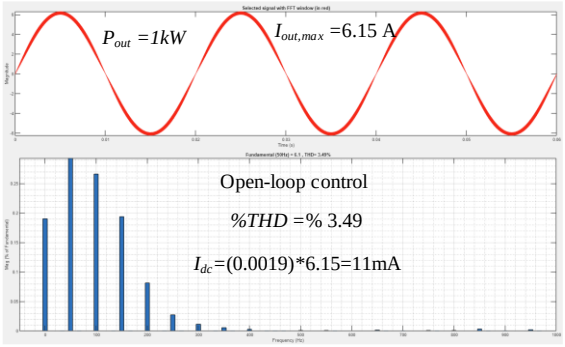


Fig. 7. FFT analysis of the output current under open-loop control condition.

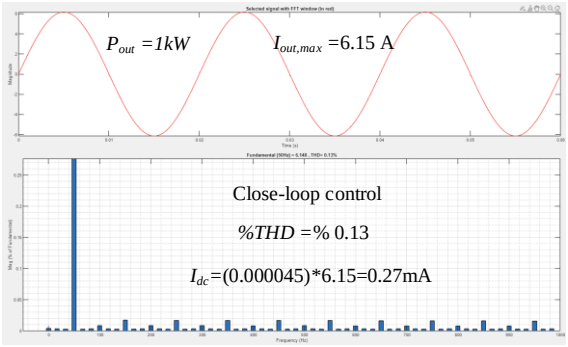


Fig. 8. FFT analysis of the output current under close-loop control condition.

However, if the converter is controlled by the close-loop control system, the DC-offset value can be greatly reduced and brought close to zero. It is also important to mention that common-

grounded converters eliminate the leakage current caused by the dissipation capacitors of the solar panels. Here, in order to show the DC-offset of the proposed converter and its elimination by the control system, a simulation was conducted. In this simulation, the input voltage is 400 V DC, the output voltage is 230 V rms, the switching frequency is 32 kHz, the value of capacitors C_1, C_2 and C_3 is equal to 22 µF, the value of the output filter inductor is equal to 0.45 mH, and the value of the output filter capacitor is equal to 1 µF. The simulation was done in two open-loop and close-loop scenarios; the FFT-analysis of the output current is shown for both scenarios.

Fig. 7 shows the FFT analysis of the output current in the open-loop control mode. In this figure, the output power is about 1 kW and the THD of the output current is 3.4%. Also, the DC-offset value of the output current is about 11 mA. In Fig. 8, the FFT analysis of the output current is shown in the output power of 1 kW and in the close-loop control mode. The THD value of the output current is equal to 0.13% and the DC-offset value is around 0.27 mA, which is a very low value. Therefore, it is concluded that the control system used in this converter has very well addressed the DC-offset problem.

VII. Comparative Study

In this part, the performance of the proposed converter is compared with several other converters in order to demonstrate the advantages and disadvantages of the proposed design. As the converters to be compared are designed on different power levels and conditions and with different power electronic devices and facilities, they cannot be compared based on the information reported in previous research. Since the converter proposed in this paper can produce both AC and DC voltage in its output, the converters used for our comparison are able to produce AC and DC voltage in their output. For a fair comparison, the compared converters were simulated in the same conditions using MATLAB/Simulink. The converters compared are described in [13]-[15], [18], and [22]-[25]. Data for the simulation are as follows: 1 kW output power, 200 V input voltage, 230 Vrms output voltage, and 30 kHz switching frequency. The internal resistance of all switches and diodes is 50 mΩ, and the internal voltage drop of the diodes is 0.7 V. By choosing 1 mH for the output filter of the proposed converter, its current ripple is about 31%. By choosing 22 µF for each of the capacitors C_1, C_2, and C_3, their voltage ripple value is around 4.2%. By considering the same current ripple for the inductors and the same voltage ripple for the capacitors of other converters, the values of the passive components were obtained, which are given in Table III.

In all the compared converters as well as in the proposed converter, the value of the output filter capacitor was chosen equal to 3.3 µF. The value of internal resistance for 1 mH inductor was considered equal to 0.2 Ω.

Table III
The Values of the Passive Components in the Compared Converters

Topologies	Values of passive components
JESTPE-[13]	L_1=0.78mH, L_f=0.1mH, C_f= 3.3µF
TIE-[14]	L_1=0.78mH, L_2=0.78mH, L_f=0.1mH, C_2=10µF, C_f=3.3µF
JESTIE-[18]	L_1=1.25mH, L_f=2.05mH, C=6µF, C_f= 3.3µF
TIE-[15]	L_m=0.74mH, L_f=0.1mH, C_f= 3.3µF
TEC-[22]	L_f=1mH, C_1=22µF, C_2=22µF, C_3=100µF, C_f=3.3µF
TPEL-[23]	L_f= 0.77mH, C_1= 4000µF, C_2= 30µF, C_f=3.3µF
TPEL-[24]	L_f= 0.75mH, C_1=2000µF, C_2=2000µF, C_f=3.3µF
RPG-[25]	L_f=0.9mH, C_1=1500µF, C_2=100µF, C_3=350µF, C_f=3.3µF

To match the internal resistance of all inductors, the following formula was used:

$$\frac{R_{new}}{R_{old}} = \sqrt{\frac{L_{new}}{L_{old}}} \tag{35}$$

In order to evaluate the volume of energy storage elements, the value of stored energy in them can be calculated. Equations (36) and (37) show the total stored energy inside the inductors and capacitors of the converters. In these formulas, the capacitor and the inductor in the output filter are also considered.

$$Vol_L \cong W_L = 0.5 \times \sum_{i=1}^{N_L} L_i \cdot I_{L,\max}^2 \tag{36}$$

$$Vol_C \cong W_C = 0.5 \times \sum_{i=1}^{N_C} C_i \cdot V_{C,\max}^2 \tag{37}$$

In the above, N_L and N_C are the number of capacitors and inductors in the converter, and I_{Lmax} and V_{Cmax} are the maximum current of the inductors and the maximum voltage of the capacitors.

To calculate the total standing voltage (*TSV*), equation (38) was used, and this parameter is based on the input voltage.

$$TSV = \frac{\sum_{i=0}^{N_D+N_S} V_i}{V_{in}} \tag{38}$$

In (38), N_D and N_S are the number of switches and diodes. Table IV shows the comparison between the proposed converter and other converters. W_L and W_C denote the total stored energy inside the inductors and capacitors of the converters. TSV shows the total standing voltage in the switches and diodes, which is based on the input voltage.

Table IV
Comparison Table Between Proposed Converter and Other Converters

Topologies	N_S	N_D	N_C	N_L	W_L (mJ)	W_C (J)	TSV (p.u.)	Boosting factor	V_{in}	V_{out} rms	P_{out} (kW)	P_{CON} (W)	MSV	Reported Efficiency
JESTPE-[13]	8	-	1	2	111.7	0.1743	13.4	d/(1-d)	200V	230V	1	41	V_{in}+V_{out}	97.5%@0.8kW
TIE- [14]	6	-	2	3	148.8	0.7024	11.13	d/(1-d)	200V	230V	1	30	V_{in}+V_{out}	97.6%@0.8kW
JESTIE- [18]	6	-	2	2	106.2	1.17	13.85	d/(1-d)	200V	230V	1	22	V_{in}+V_{out}	97.8%@1.5kW
TIE- [15]	10	-	1	2	106.3	0.1743	14.375	d/(1-d)	200V	230V	1	46	V_{in}+V_{out}	94.2%@0.3kW
TEC- [22]	6	3	4	1	18.9	10.2	18	2	200V	230V	1	32	2V_{out}	97.9%@0.5kW
TPEL- [23]	9	-	3	1	14.6	80.6	11	2	200V	230V	1	25	V_{out}	97.2%@0.6kW
TPEL- [24]	7	2	3	1	14.2	164	17	2	200V	230V	1	35	2V_{out}	98.1%@0.6kW
RPG- [25]	6	3	4	1	17	66	19	2	200V	230V	1	29	2V_{out}	97.5%@0.7kW
Proposed	9	3	4	1	18.9	2.81	14	4	200V	230V	1	26	V_{out}	98%@1.3kW

The parameter of the boosting factor shows the voltage gain of the converters and finally, P_{CON} gives the total conduction losses of the converters and MSV indicates the maximum switching voltage of the converters. The topologies in [13], [14], and [15] are based on flying inductors and the topology in [18] is based on flying capacitor technologies. In the topologies of [13], [14], and [15], the process of power transfer from the input source to the grid or the output load is monitored by charging and discharging the inductor. Although converters in [13] and [14] have fewer switches than the proposed converter, the conduction losses in these converters are higher than in the proposed converter. Also, even though these converters have lower total capacitor stored energy and *TSV* than the proposed converter, the value of stored energy inside the inductors of the converters in [13] and [14] is much higher than that of the proposed converter. The converter in [18] has less losses and fewer switches than the proposed converter, and the value of stored energy in the capacitor is half of that of the proposed converter, but the value of stored energy in the inductor of the converter in [18] is much higher than that of the proposed converter. It is important to mention that another part of inductor losses is related to core losses, which are not considered here. The presence of core losses brings about an increase in the converter losses in [18]. In terms of *TSV*, both converters are almost the same, so that the *TSV* of the proposed converter is slightly higher than that of the converter in [18]. The value of the capacitor stored energy of the converter in [15] is lower compared to the proposed converter. This converter does not have a diode; instead, the conduction losses and the *TSV* of that converter are higher than those of the proposed converter. The value of stored energy in the inductor in this converter is much higher than that of the proposed converter. Finally, this converter has fewer diodes and one more switch than the proposed converter. The topologies in [22]- [25] are based on the SC technology and power is transferred from the input source to the output side by the capacitors.

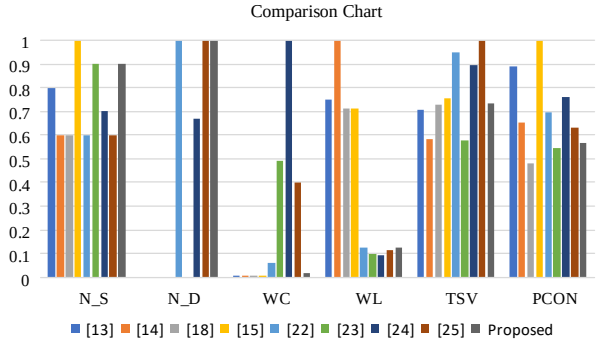


Fig. 9. Comparison of the proposed converter and other converters.

The topologies in [22], [24], and [25] have fewer switches than the proposed converter; in converters [23] and [25], the value of the stored energy in the inductor is lower than that of the proposed converter. However, these converters have higher conduction losses, the voltage gain is lower, and the *TSV* is higher than that of the proposed converter. Also, in these converters, the stored energy in the capacitors is higher than that of the proposed converter. Finally, the converter in [23] has no diode and a lower *TSV* than the proposed converter. It also has about 1 W less conduction losses and about 4.9 mJ lower inductor stored energy than the proposed converter. Instead, the proposed converter has twice the voltage gain compared to the converter in [23] and the capacitor stored energy in the converter in [23] is much higher than in the suggested converter. Fig. 9 shows a bar graph to compare the proposed converter with other converters and provide a better understanding of its advantages and disadvantages. The information in this chart is extracted from Table IV.

The number of capacitors (N_C) and inductors (N_L) in each converter has been added to the comparison table. Although the proposed converter has four capacitors (taking into account the output filter capacitor for all converters), the total amount of energy stored in the capacitors is lower than in all the switch-capacitor converters [22]-[25], which is the reason of the low capacity of the capacitors in the proposed converter. The capacity of the capacitors used for each converter in the comparison section is given in Table III. The converters in Table IV are completely made in different conditions with different output power. In reference [15], the output power is 0.3 kW, in references [22], [24], [25], the power is around 0.7 kW and without PCB, made on ready-made boards, while the proposed converter is made for 4 kW/7kW power, and the PCB is designed for it. Therefore, it is not possible to compare the converters in Table IV in terms of cost of materials and overall size. Even in the case of the same power level, it is very difficult to provide fair cost analysis as it depends on the supply chain and logistics. In the following, the volume of the proposed converter and its power density are calculated. Also, the reported efficiency of each of the converter is given in Table IV. In order to calculate the power density of the proposed converter, it is necessary to calculate the volume of the energy storage elements as well as the volume of the heatsink:

$$Volume\_Heatsink = L \times W \times H = 240 \times 200 \times 40 = 1924\ cm^3 \tag{39}$$

$$Volume\_L_f = 9.4 \times 8.1 \times 2.8 = 213.19\ cm^2 \tag{40}$$

$$Volume\_C_{1,2,3} = 3 \times (4.1 \times 2.2 \times 3.6) = 97.41\ cm^3 \tag{41}$$

$$Volume\_C_f = 3.15 \times 1.5 \times 2.45 = 11.57\ cm^3 \tag{42}$$

The total volume of the converter is calculated from the following equation:

$$Total\_Volume = 1924 + 213.19 + 97.41 + 11.57 = 2246.17\ cm^3 \tag{43}$$

Finally, the power density of the prototype is calculated as follows:

$$Power\ Density = \frac{P_{out}}{Total\_Volume} = \frac{7000}{2246.17} = 3.116\ W/cm^3 \tag{44}$$

VIII. Experimental Results

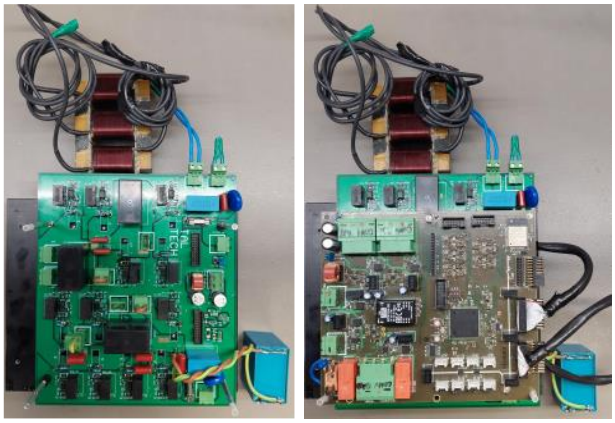
In this section, several experimental results are presented to validate the performance of the proposed inverter. To control and generate PWM pulses for the switches, the TMS320F28379D series microcontroller from Texas Instrument was used. All the voltage and current sensors, the isolator between the microcontroller and the gate drivers, as well as the MCU unit are

placed in one board. Fig. 10 shows the designed experimental setup. In order to feed the power circuit, programmable DC power supply Chroma 62150H-1000s was used. For efficiency measurements of the proposed inverter in different conditions, a YOKOGAWA-WT1806E power analyzer was applied. A Tektronix MDO4034B-3 oscilloscope was employed to measure and display the required results. All the switches, gate drivers, gate driver power supply, output filter, and the value of the capacitors are shown in Table V. Instead of conventional diodes, active diodes are used. The output of the inverter uses an *LC* filter instead of an *L* filter. Fig. 11(a) shows the 9-level inverter output voltage, load voltage, load current, and input current. In this figure, the input voltage value is equal to 100 V, and the peak output voltage equals 400 V. Therefore, this proposed topology produces four times higher voltage gain. The peak voltage of the load is equal to 325 V and the peak current of the load equals 4 A, so the power is 0.65 kW. Fig. 11(b) shows the voltage of each of the capacitors C_1, C_2, and C_3. According to this figure, the capacitor C_1 is charged as much as the input voltage, the capacitor C_2 is charged twice the input voltage, and the capacitor C_3 is charged four times the input voltage.

TABLE V
PARAMETERS OF THE PROPOSED UNIVERSAL CONVERTER

Parameters	Value
Output voltage in dc-ac/dc-dc	230 V rms/ 350 V dc
Output power	3.78 kW(dc-ac)/ 7 kW(dc-dc)
Switching frequency	32 kHz
Output filter inductor L_f	0.45 mH
Output filter capacitor	3.3 µF
Power switches	C3M0030090K
Capacitor C1	0.56 mF in multi-level, 22 µF in three-level
Capacitor C2	1.12 mF in multi-level, 22 µF in three-level
Capacitor C3	1.36 mF in multi-level, 22 µF in three-level
Gate driver power supply	MGJ2D121505SC
Gate drivers	ACPL-H342

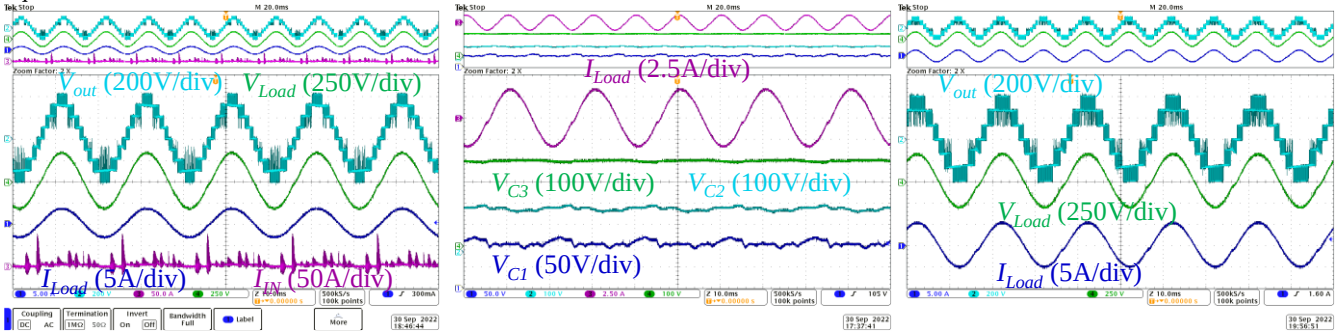
As the proposed converter is SC-based, there is no need for an additional controller to control the voltage of the capacitors. In addition, along with the voltage of the capacitors, this figure shows the output current. Fig. 11(c) illustrates the performance of the proposed converter in the seven-level mode where the output voltage of the inverter, the load voltage along with the load current are shown. The input voltage is equal to 135 V, and the output power equals 0.8 kW.



(a) (b)

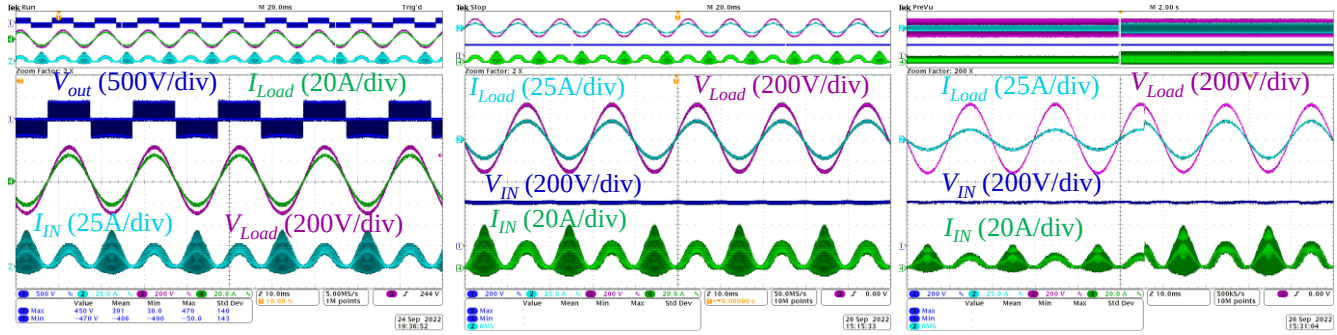
Fig. 10. (a) Power board of the experimental setup, (b) control board of the experimental setup.

Fig. 12(a) shows the performance of the proposed inverter in the three-level working mode. Since the frequency of charge and discharge of capacitors C_1, C_2, and C_3 is equal to the switching frequency, it results in a low value of the capacitor. In this figure, the output voltage of the inverter, the voltage and current of the load, as well as the input current are provided. The input voltage is 400 V, and the output power is 3.78 kW. It should be noted that at 3.78 kW, the value of each of the capacitors is equal to 22µF. Fig. 12(b) shows the voltage and current of the load along with the input voltage and current of the inverter. In this figure, the input voltage is equal to 400 V, and the output power equals 3.78 kW. Fig. 12(c) shows the performance of the proposed inverter in the condition of a step change in the output load. In this figure, the output load has been changed from 1.8 to 3.6 kW, and it can be seen that the performance of the inverter is stable under step change conditions. In Fig. 12(c), the input voltage is equal to 400V. Fig. 13(a) and (b) show the performance of the proposed converter at other input voltages. These two figures show the load voltage and current along with the input voltage and current. In Fig. 13(a), the input voltage is equal to 200 V, and the output power equals 2 kW. Furthermore, in this working mode, only capacitors C_1 and C_3 are in the path of the current and output power, the capacitor C_2 is disconnected, and the voltage gain is equal to two.



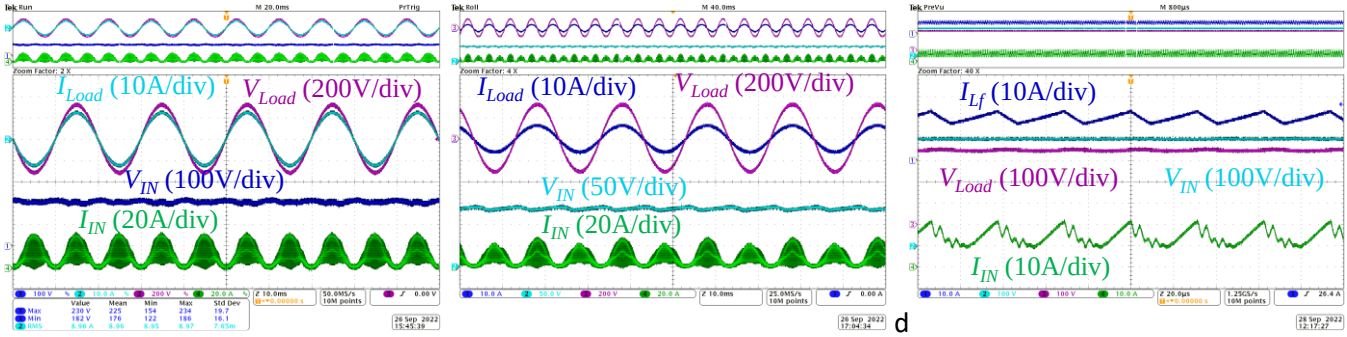
(a) (b) (c)

Fig. 11. (a) The nine-level output voltage of the inverter, load voltage and current, and input current in the output power at 0.65 kW and 200 V input voltage, (b) the voltage across capacitors C1, C2, C3 along with the load current, (c) the seven-level output voltage along with the load voltage and current at 0.8 kW and input voltage of 135 V.



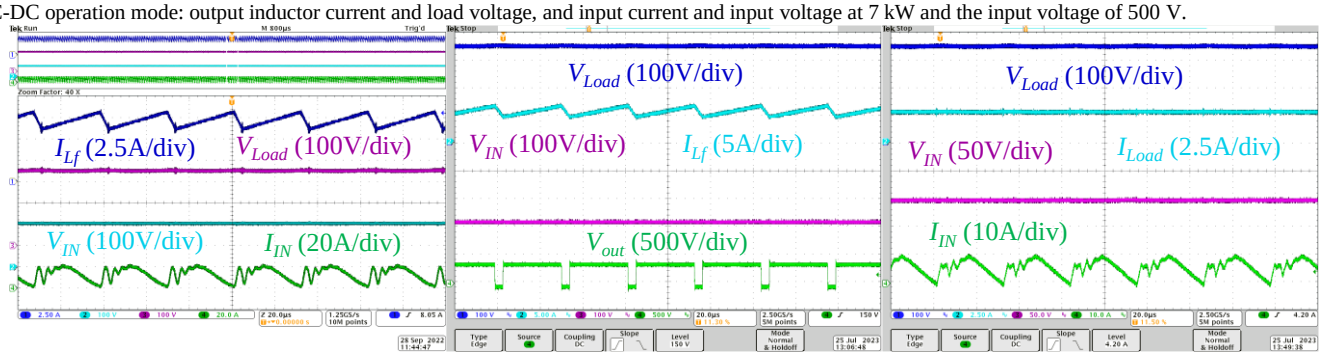
(a) (b) (c)

Fig. 12. (a) The output voltage of the inverter, load voltage and current, and input current at 3.78 kW and 400 V input voltage, (b) load voltage and current, and input voltage and current at 3.78 kW and input voltage of 400 V, (c) load voltage and current, and input voltage, and current in the step-change condition from 1.8 kW to 3.6 kW.



(a) (b) (c)

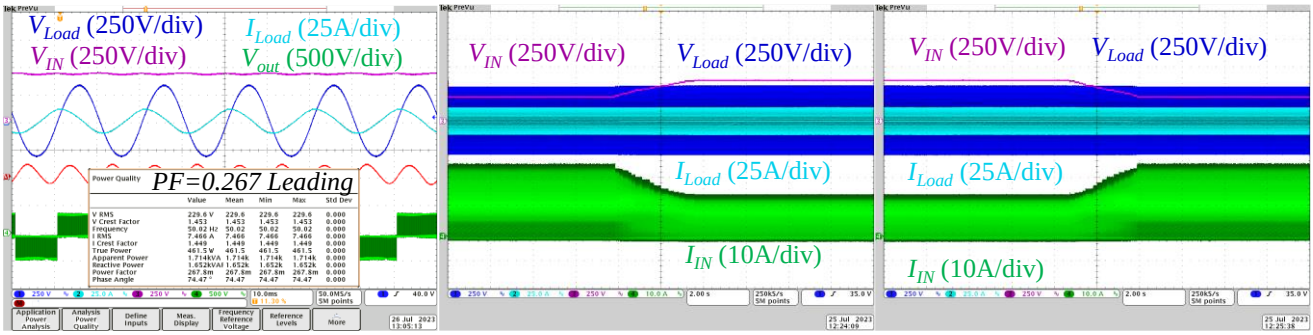
Fig. 13. The load voltage and current, and the input voltage and current: (a) at 2 kW and with the input voltage of 200 V, (b) at 1.13 kW and the input voltage of 135 V (c) DC-DC operation mode: output inductor current and load voltage, and input current and input voltage at 7 kW and the input voltage of 500 V.



(a) (b) (c)

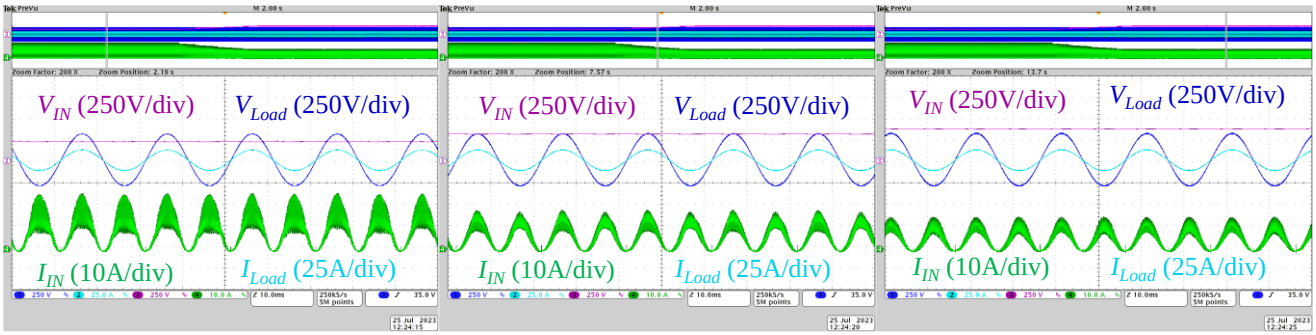
Fig. 14. DC-DC operation modes, input voltage and load voltage: (a) input current and output inductor current with the input voltage of 200 V, the load voltage of 350 V and the output power of 2.49 kW, (b) output voltage V_{out} before the LC filter, and output inductor current, with the input voltage of 200 V, the load voltage of 350 V, and the output power of 1.75 kW, (b) input current and load current with the input voltage of 150 V, the output voltage of 350 V and the output power of 0.9 kW.

In Fig. 13(b), the input voltage is equal to 135 V and the output power equals 1.13 kW. The voltage gain in this working mode is equal to three and all the capacitors are in the output power path. Since the converter in this study is proposed for DC-AC and DC-DC applications, it is necessary to show its performance in the DC-DC mode. For this purpose, Fig. 13(c) demonstrates the correct operation of the converter in the DC-DC working mode. In this figure, the input voltage and the current of the converter are shown along with the output voltage and the current of the output inductor. The input voltage is 500 V and the output voltage is 350 V. Since the output current is equal to the average value of the output filter inductor current, it can be concluded from Fig. 13(c) that the output load current is equal to 20 A. DC output current with an average value of 20 A and output voltage of 350 V results in an output power of 7 kW. Therefore, the power in Fig. 13(c) is equal to 7 kW. Fig. 14(a) shows the experimental result in the DC-DC condition with 200 V input voltage, 350 V output load voltage, and 2.49 kW output power. In this figure, the input voltage and current are shown along with the load voltage and output inductor current. Since the average value of the load current is equal to the average value of the output inductor current, according to the blue figure, the average value of the output inductor current is around 7.1 A. As a result, for the load voltage of 350 V, the output power is 2.49 kW. Fig. 14(b) shows the output voltage V_{out} before the LC filter. In this figure, the input voltage, load voltage, output voltage V_{out}, and output inductor current I_{Lf} are shown. The average output current equals 5 A, and at the load voltage of 350 V, the output power value equals 1.75 kW. Fig. 14(c) is given shows the voltage boosting capability of the proposed converter in the DC-DC mode to the best possible extent where the input voltage equals 150 V, the load voltage equals 350 V, and the output power equals 0.9 kW.



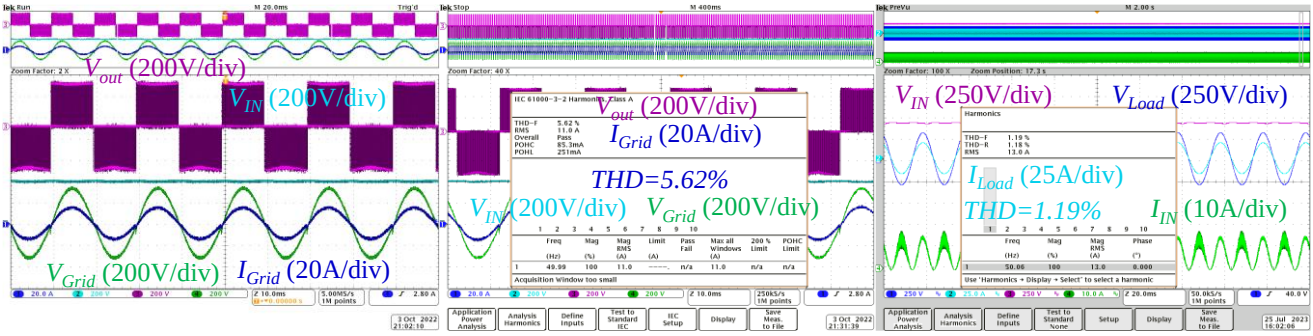
(a) (b) (c)

Fig. 15. (a) Non-unity power factor mode: load voltage and current, output voltage and input voltage at the output power of 1.71 kVA, the power factor of 0.267 Leading, and at the input voltage of 400 V, the input voltage and current, and the load voltage and current at the output power of 2.2 kW: (b) during the transition at the input voltage from 200 to 350 V, (c) during the transition at the input voltage from 350 to 200 V.



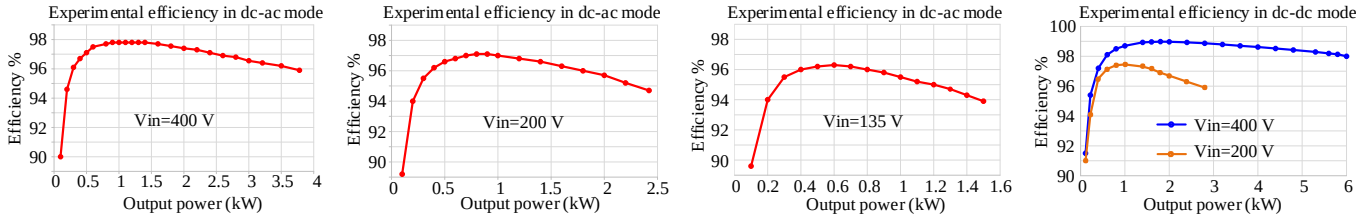
(a) (b) (c)

Fig. 16. Zoomed mode of Fig. 15(b) during the transition in the input voltage and at the output power of 2.2 kW: (a) input voltage is lower than the peak value of the load voltage (b) input voltage is equal to the peak value of the load voltage, and (c) input voltage is higher than the peak value of the load voltage.



(a) (b) (c)

Fig. 17. DC-AC in the grid-connected condition: input voltage, grid voltage and current, and output voltage (a) with the input voltage of 400 V, the grid voltage of 230 Vrms, and the output power of 2.53 kW, (b) grid injected current with the THD of 5.62% and the output power of 2.53 kW, (c) the THD of the output load current in the local load conditions, with the input voltage of 400 V, the output power of 2.99 kW, and the THD of 1.19% for load current.



(a) (b) (c) (d)

Fig. 18. Experimental efficiencies in DC-AC modes: (a) with the input voltage of 400 V, (b) with the input voltage of 200 V, (c) with the input voltage of 135 V, (d) experimental efficiency in the DC-DC mode with the input voltage of 200 V and 400 V.

Therefore, it can be concluded from Fig. 14 that the proposed converter, in addition to the DC-AC operating mode, also has the ability to increase the voltage in the DC-DC operating mode.

In order to show the ability of the proposed converter to control and support the reactive power, the experimental result is given in the leading power factor mode, which can be created by the RC load at the output of the inverter. Fig. 15(a) shows the input voltage, the output load voltage and current, and the voltage of the inverter. In this figure, the input voltage is 400 V, the output apparent power is 1.71 kVA, the active power is 0.46 kW, and the

output reactive power is 1.65 kVAR. The output leading power factor is equal to 0.267. For this amount of the power factor, the phase difference between the output load voltage and the current is equal to 74.47 degrees. This value of the output power factor means that the proposed converter is able to control the reactive power at lower power factors.

Fig. 15(b) demonstrates the performance of the proposed converter for changes in the input DC voltage. In this figure, the input voltage and current, as well as the load voltage and current are shown. In order to demonstrate the stability of the proposed converter, changes were applied to the input voltage, which increased from 200 to 350 V. In Fig. 15(b), despite the changes in the input voltage, the load voltage and current are kept constant by the control system. Therefore, in the process of changing the input voltage, the output load power is constant and is equal to 2.2 kW. The constant of the output power has caused the input current to decrease when the input voltage increases. In the case of a grid-connected solar system, the behavior will be different, but these tests show the ability of performance with changing input voltage. In Fig. 15(c), the input voltage changes from 350 to 200 V, while the output voltage, current and output power remain constant, and the converter maintains its stability. Fig. 16 shows the zoomed state of Fig. 15(b) at three different points. In Fig. 16(a), the input voltage is lower than the peak value of the load voltage; in Fig. 16(b), the input voltage is equal to the peak value of the output load voltage, and in Fig. 16(c), the input voltage is higher than the peak of the output load voltage. According to these figures, despite the changes in the input voltage, the voltage and current of the output load are constant, which indicates proper operation of the control system and stability of the converter. Fig. 17(a) shows the result of the proposed converter in the DC-AC mode and when the converter is connected to a single-phase grid with the voltage of 230 Vrms and frequency of 50 Hz. This figure shows the input voltage, grid voltage and injected current into the grid, and output voltage of the inverter. The value of the input voltage is equal to 400 V and the injected power to the grid is 2.53 kW. According to Fig. 17(a), the output voltage of the inverter is well synchronized with the grid, and the proposed converter works in grid-connected or grid-following conditions. The THD of the output current in both grid-connected and local load conditions was measured by Tektronix MDO4034B-3 oscilloscope. Fig. 17(b) shows the THD of the output current of the proposed converter in the grid-connected mode. According to this figure, the THD of the injected current to the grid is around 5.62%. This value is acceptable for inverters connected to the grid. Also, in Fig. 17(c), the THD of the load current is shown. According to this figure, the THD of the output current in the load condition is around 1.19%. The output AC current with a THD value of about 1.19% is a current with good quality for the output loads of the converter. In Fig. 18, the proposed converter is investigated in terms of experimental efficiency, and the practical efficiency at different operating points is given. It is important to mention that all the data in Fig. 18 were measured directly by the power analyzer. In Fig. 18(a)-(c), the proposed converter is in the DC-AC working mode. The input voltage in Fig. 18(a)-(c) is 400 V, 200 V, and 135 V, respectively. According to these figures, the maximum efficiency is 98% at 400 V, 97% at 200 V, and 96% at 135 V input voltage. Also, experimental efficiency in the DC-DC working mode is presented in Fig. 18(d). In this figure, two efficiency curves are given for the input voltages of 200 V and 400 V. Fig. 18(d) shows that the maximum efficiency is 97.5% for the 200 V input voltage and 99% for the 400 V input voltage.

IX. Conclusion

In this paper, a new power electronic interface based on SC was presented. The proposed converter is common grounded, which eliminates the leakage current in photovoltaic systems and increases the safety of the system. The ability to boost four times the input voltage makes the proposed converter capable of supplying the loads at input voltages lower than the peak value of the output voltage without the need of an additional boost converter. An explanation of the operating modes as well as the design of the values of the passive components were provided. A comparison was made between the proposed converter and other converters in order to evaluate the pros and cons of the proposed converter. The experimental efficiency curves were shown for different input voltages and in two states, DC-DC and DC-AC, with all these curves directly extracted from the power analyzer. Finally, to show the accurate operation of the proposed converter, experimental results were presented in the DC-AC and the DC-DC working modes and at power levels of 3.78 kW and 7 kW, which is not typical for SC solutions. In turn, it demonstrates the feasibility of such approaches for industrial applications. Due to the minor presence of magnetic materials and corresponding conduction losses, a very flat efficiency curve can be achieved. To increase the lifespan of switched-capacitor converters and to use them at higher power levels, it is recommended to use a converter in which the capacitors can be charged and discharged at the switching frequency. In this way, low-value capacitors can be used, with film capacitors being a suitable option for this purpose.

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References

[1] J. Nan, Wei Yao, Jinyu Wen, “Energy storage-based control of multi-terminal DC grid to eliminate the fluctuations of renewable energy,” *The Journal of Engineering*. vol. 16, no. 3, pp. 991- 995, 2019.

[2] L. Zhang, K. Sun, Y. Xing, L. Feng, H. Ge, ‘A modular grid connected photovoltaic generation system based on DC bus’. *IEEE Trans. on Power Electron.*, vol. 26, no. 2, pp. 523–531, 2011.

[3] P. Bauer, ‘Roadmap for DC’, *EPE'20 ECCE Europe*, 2020.

[4] S. Rivera, R. Lizana, S. Kouro, T. Dragičević, B. Wu, “Bipolar DC Power Conversion: State-of-the-Art and Emerging Technologies,” *IEEE Journal of Emerge. Selected Topics. Power. Electron*, vol. 21, no. 9, pp. 1192 - 1204, 2021.

[5] A. Sannino, G. Postiglione, and M. H. J. Bollen, “Feasibility of a DC network for commercial facilities,” *Industry Applications, IEEE Trans. on*, vol. 39, no. 5, pp. 1499– 1507, 2003.

[6] D. Boroyevich, I. Cvetkovic, D. Dong, R. Burgos, Fei Wang, and F. Lee, “Future electronic power distribution systems a contemplative view,” *in proc. of Optimization of Electrical and Electronic Equipment (OPTIM)*, 2010 12th International Conference on, 2010, pp. 1369–1380.

[7] https://dc-foundation-netherlands.org/wp-content/uploads/2019/05/3.5-GG-DC-congres-15-6-2018-presentatie-Joost-de-Koning-V1.pdf

[8] O. Husev, O. Matiushkin, D. Vinnikov, C. Roncero-Clemente, S. Kouro, "Novel Concept of Solar Converter with Universal Applicability for DC and

AC Microgrids," *IEEE Tran. on Ind. Electron*., vol. 69, no. 5, pp. 4329 - 4341, 2022.

[9] O. Husev, D. Vinnikov, S. Kouro, F. Blaabjerg and C. Roncero-Clemente, "Dual-Purpose Converters for DC or AC Grid as Energy Transition Solution: Perspectives and Challenges," *in IEEE Industrial Electronics Magazine*, (Early access), 2023.

[10] D. Salomonsson, L. Soder, A. Sannino, "Protection of Low-Voltage DC Microgrids", *IEEE Trans. on Power Delivery*, vol. 24, no. 3, pp. 1045 - 1053, 2009.

[11] D. Paul, "DC traction power system grounding, "*IEEE Trans. Ind. Appl*., vol. 38, no. 3, pp. 818–824, May/Jun. 2002.

[12] IEEE Recommended Practice for the Design of DC Auxiliary Power Systems for Generating Stations, IEEE Std. 946-2004, 2004.

[13] N. V. Kurdkandi, O. Husev, O. Matiushkin, D. Vinnikov, Y. P. Siwakoti and S. S. Lee, "Novel Family of Flying Inductor-Based Single-Stage Buck–Boost Inverters," *IEEE Journal of Emerge. Selected Topics. Power. Electron.*, vol. 10, no. 5, pp. 6020-6032, Oct. 2022.

[14] O. Husev, N. V. Kurdkandi, M. G. Marangalu, D. Vinnikov and S. H. Hosseini, "A New Single-Phase Flying Inductor-Based Common Grounded Converter for Dual-Purpose Application," *IEEE Trans. Ind. Electron*., vol. 70, no. 8, pp. 7913-7923, Aug. 2023.

[15] M. T. Azary, M. Sabahi, E. Babaei and F. A. Aghdam Meinagh, "Modified Single-Phase Single-Stage Grid-Tied Flying Inductor Inverter with MPPT and Suppressed Leakage Current," *IEEE Trans. on Ind. Electron.*, vol. 65, no. 1, pp. 221-231, Jan. 2018.

[16] O. Matiushkin, O. Husev, J. Rodriguez, H. Young, I. Roasto, "Feasibility Study of Model Predictive Control for Grid-Connected Twisted Buck-Boost Inverter," *IEEE Trans. Ind. Electron.*, vol. 69, no 3, pp. 2488 - 2499, March. 2022.

[17] N. V. Kurdkandi, O. Husev, S. Rahimpour, C. Roncero-Clemente, O. Matiushkin and D. Vinnikov, "A Novel Flying Inductor based Grid-Connected Inverter with Buck-Boost Ability," *IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium, 2022, pp. 1-6.*

[18] T. H. Shahsavar, N. V. Kurdkandi, O. Husev, E. Babaei, M. Sabahi, A. Khoshkbar-Sadigh, D. Vinnikov, "A New Flying Capacitor-Based Buck–Boost Converter for Dual-Purpose Applications," *IEEE J. of Emerging and Selected Topics in Ind. Electron.*, vol. 4, no. 2, pp. 447-459, April 2023.

[19] Y. P. Siwakoti and F. Blaabjerg, "Common-Ground-Type Transformerless Inverters for Single-Phase Solar Photovoltaic Systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2100-2111, March 2018.

[20] J. F. Ardashir, M. Sabahi, S. H. Hosseini, F. Blaabjerg, E. Babaei and G. B. Gharehpetian, "A Single-Phase Transformerless Inverter With Charge Pump Circuit Concept for Grid-Tied PV Applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5403-5415, July 2017, doi: 10.1109/TIE.2016.2645162.

[21] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, "Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793-805, Feb. 2013.

[22] N. V. Kurdkandi, M. G. Marangalu, S. S. Vala, P. Mohseni, A. Z. Gharehkoushan, S. H. Hosseini, M. Sabah "A New Transformer-Less Common Grounded Three-Level Grid-Tied Inverter With Voltage Boosting Capability," *IEEE Tran. Energy Conversion*, vol. 36, no. 3, pp. 1896-1909, Sept. 2021.

[23] R. Barzegarkhoo, S. S. Lee, S. A. Khan, Y. P. Siwakoti, and D. D. Lu, "A Novel Generalized Common-Ground Switched-Capacitor Multilevel Inverter Suitable for Transformerless Grid-Connected Applications," *IEEE Trans. Power Electron*., vol. 36, no. 9, pp. 10293- 10306, Sep. 2021.

[24] R. Barzegarkhoo, Y. P. Siwakoti and F. Blaabjerg, "A New Switched-Capacitor Five-Level Inverter Suitable for Transformerless Grid-Connected Applications," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8140-8153, Aug. 2020.

[25] N. V. Kurdkandi, M. G. Marangalu, P. Alavi, A. Z. Gharehkoushan, S. Rahimpour, M. R. Islam, K. M. Muttaqi, "A new transformer-less common grounded five-level grid-tied inverter with leakage current elimination and voltage boosting capability for photovoltaic applications," *IET Renew. Power Gener*. 1–26 (2023).

[26] N. V. Kurdkandi, M. G. Marangalu, S. Mohammadsalehian, H. Tarzamni, Y. P. Siwakoti, M. R. Islam, K. M. Muttaqi, "A New Six-Level Transformer-Less Grid-Connected Solar Photovoltaic Inverter with Less Leakage Current," *in IEEE Access*, vol. 10, pp. 63736-63753, 2022.

[27] N. V. Kurdkandi, M. G. Marangalu, O. Husev, A. Aghaie, M. R. Islam, Y. P. Siwakoti, K. M. Muttaqi, S. H. Hosseini "A New Seven-Level Transformer-Less Grid-Tied Inverter with Leakage Current Limitation and Voltage Boosting Feature," *IEEE J. of Emerg. and Selected Topics in Ind. Electron.*, vol. 4, no. 1, pp. 228-241, Jan. 2023.

[28] O. Husev, C. Roncero-Clemente, E. Makovenko, S. Pires Pimentel, D. Vinnikov, J. Martins, "Optimization and Implementation of the Proportional-Resonant Controller for Grid-Connected Inverter with Significant Computation Delay," *IEEE Trans. on Ind. Electron*, vol. 67, no 2, pp. 1201 - 1211, Feb. 2020.

[29] O. Husev, J. Belikov, O. Matiushkin, D. Vinnikov, R. Ahmadiahangar, N.V. Kurdkandi, "Optimal Tuning of Resonant and Repetitive Based Controller for Single-Phase Buck-Boost Inverter with Unfolding Circuit". *IEEE Journal of Emerg. Sel. Top. Ind. Electron.* 2021, Early access.

[30] J.-K. Kim, J.-H. Lee, H.-G. Jeong, and K.-B. Lee, "Improvement of gridconnected inverter systems with PR controllers under the unbalanced and distorted grid voltage," in *Proc. IEEE 7th Int. Power Electron. Motion Control Conf.*, 2012, pp. 1183–1187.

[31] Y. Yang, L. Hadjidemetriou, F. Blaabjerg, and E. Kyriakides, "Benchmarking of phase locked loop based synchronization techniques for gridconnected inverter systems," in *Proc. IEEE Int. Conf. Power Electron.*, 2015, pp. 1–8.

[32] M. A. G. de Brito, L. Galotto, L. P. Sampaio, G. A.Melo, and C. A. Canesin, "Evaluation of the main mppt techniques for photovoltaic applications," *IEEE Trans. Ind. Electron*., vol. 60, no. 3, pp. 1156–1167, Mar. 2013.

[33] E. Kabalci, "The design and analysis of a two-stage PV converter with Quasi-Z source inverter," in *Proc. IEEE 18th Int. Power Electron. Motion Control Conf.*, 2018, pp. 451–456.

[34] I. Grgi´c, M. Baši´c, and D. Vukadinovi´c, "Optimization of electricity production in a grid-tied solar power system with a three-phase quasi-Z-source inverter," *J. Cleaner Prod.*, vol. 221, pp. 656–666, 2019.

[35] M. Aureliano Gomes de Brito, L. Galotto, L. Poltronieri Sampaio, G. de Azevedo e Melo, and C. Alberto Canesin, "Evaluation of the main MPPT techniques for photovoltaic applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 1156–1167, Mar. 2013.

[36] H. Khoun Jahan, M. Abapour and K. Zare, "Switched-Capacitor-Based Single-Source Cascaded H-Bridge Multilevel Inverter Featuring Boosting Ability," in *IEEE Trans. on Power Electron.*, vol. 34, no. 2, pp. 1113-1124, Feb. 2019.

[37] F. Akbar, A. Elkhateb, H. F. Ahmed, A. A. Khan, H. Cha and J. -W. Park, "Single-Phase Virtual-Ground Transformerless Buck–Boost Inverters," *in IEEE Trans. on Power Electron*, vol. 38, no. 9, pp. 11585-11600, Sept. 2023.

[38] I. Harbi, M. Ahmed, C. M. Hackl, J. Rodriguez, R. Kennel and M. Abdelrahem, "Low-Complexity Dual-Vector Model Predictive Control for Single-Phase Nine-Level ANPC-Based Converter," in *IEEE Trans on Power Electron.*, vol. 38, no. 3, pp. 2956-2971, March 2023.

[39] M. Hazrati-Karkaragh, M. Esteki, M. R. Mohammadi and S. A. Khajehoddin, "A Novel High-Frequency Inverter With ZVT in a Wide Range of Duty Cycles and PFs," *in IEEE Trans on Power Electron*, vol. 38, no. 8, pp. 9983-9997, Aug. 2023.