Letters

An Improved Soft-Switching Buck Converter With Coupled Inductor

Lei Jiang, Chunting Chris Mi, Siqi Li, Chengliang Yin, and Jinchuan Li

***Abstract*—This letter presents a novel topology for a buck dc–dc converter with soft-switching capability, which operates under a zero-current-switching condition at turn on and a zero-voltage-switching condition at turn off. In order to realize soft switching, based on a basic buck converter, the proposed converter added a small inductor, a diode, and an inductor coupled with the main inductor. Because of soft switching, the proposed converter can obtain a high efficiency under heavy load conditions. Moreover, a high efficiency is also achieved under light load conditions, which is significantly different from other soft-switching buck converters. The detailed theoretical analyses of steady-state operation modes are presented, and the detailed design methods and some simulation results are also given. Finally, a 600 W prototype is built to validate the theoretical principles. The switching waveforms and the efficiencies are also measured to validate the proposed topology.**

***Index Terms*—Buck converter, coupled inductor, soft switching, zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

BUCK converters, as the basic kind of dc–dc converters, have been used in many areas, such as consumer electronics, appliances, general industries, and aerospace. With technological developments, the demand for small size, lightweight, and high reliability for dc–dc converter increases sharply. High switching frequency can be used to reduce sizes and weights of converters. However, if converters work under hard-switching conditions, switching losses will increase as switching frequency increases, and the total efficiencies will drop. Soft-switching technologies are the best methods to reduce switching losses, and improve efficiencies and reliabilities. Thus, the sizes of heat sinks can be reduced. The total sizes and weights of converters will also be reduced.

There are many methods to realize soft switching, and the most common is using additional quasi-resonant circuits [1]–[10]. By adding auxiliary switches, inductors, and capacitors, zero-current-switching (ZCS) conditions or zero-voltage-switching (ZVS) conditions can be easily achieved in quasi-resonant converters. However, high voltage stresses and high current stresses for power switches are also generated [2], [3]. It is not beneficial to select the proper rank of power switches, because there are more conduction losses when using higher voltage power switches. In addition, in some converters, auxiliary switches work under hard-switching conditions [8], or work two times in a switching cycle [9]. Thus, additional power losses will be generated. Due to auxiliary switches, the control method is more complicated than that of conventional pulsewidth modulation converters, and additional measuring circuits of voltage and current are needed.

Adopting interleaved structures is also a method to realize ZVS conditions. Several conventional synchronous dc–dc converters are connected in parallel to constitute interleaved structures [11], where inductor current of each phase flows in bidirectional directions (positive and negative). When the inductor current becomes negative, the energy stored in the inductor will discharge and charge the snubber capacitors, and if the stored energy in the inductor is not enough, ZVS conditions will not be achieved. However, the current ripple of each phase is very large. To alleviate this problem, multiphase interleaved structures can be used. For example, three phases and four phases are popular. As an effective improvement, two-phase inductors are coupled with the same magnetic core to reduce the iron core loss, size, and cost of the converter [12]. In multiphase interleaved structures, there are many components such as switches and inductors, so the control algorithm is also very complex, and the cost is usually high.

Additionally, coupled inductors can also be utilized to achieve ZVS conditions [13]–[20]. By adding an auxiliary winding with the main inductor, another power flow channel is supplied to achieve soft-switching conditions. In [13], only a diode and an auxiliary winding are added to achieve ZVS conditions. It can resolve the reverse recovery problem of the body diode of the synchronous MOSFET switch. In [14], an auxiliary winding coupled with the main inductor, a small inductor, and two large capacitors are added to achieve ZVS. Its current ripple can be zero. In another ZVS converter [18], by adding a small inductor, a diode, and an auxiliary winding coupled with the main inductor, the current of the small inductor is bipolar; that is critical for ZVS. Its principle for ZVS is similar to that of interleaved structures [11]. Moreover, both interleaved structures and coupled inductors are also used to yield better results in soft-switching topologies [12], [20].

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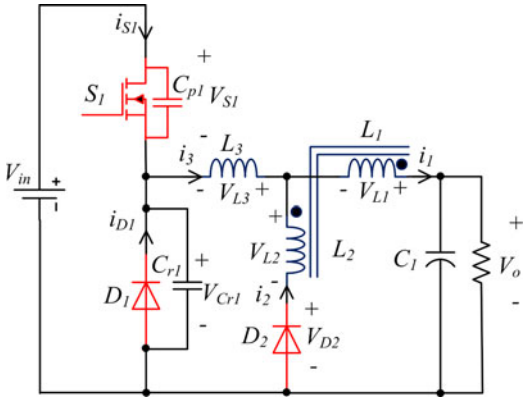

Fig. 1. Topology of the proposed ZCS–ZVS buck converter.

In most soft-switching converters, efficiencies can be improved greatly under heavy load conditions, but the effects are not good under light load conditions. It is usually because of additional power dissipations of auxiliary circuit branches. In [18], no matter how much the load is, the current waveform of the branch of the auxiliary coupled inductor is always the same. It means that the power dissipation of this branch exits and remains constant all the time, which is not beneficial for efficiency optimization at a light load.

In this letter, to solve the low-efficiency problem at a light load, based on a ZVS converter [18], an improved soft-switching buck converter is proposed. The auxiliary circuit consists of an inductor coupled with the main inductor, a small inductor, as well as a diode. The main MOSFET can operate under a ZCS condition at turn on, and a ZVS condition at turn off. The current of the small inductor is discontinuous. A converter prototype rated at 600 W is built to verify the principles.

The rest of this letter is organized as follows. In Section II, the converter topology and its detailed operating principles of each mode are presented. The design methods of the main circuit and some simulation results are given in Section III. Section IV focuses on the experimental results and analyses. Finally, the conclusion is drawn in Section V.

II. Converter Topology and Operating Principles

A. Description of the Proposed Converter

The proposed buck converter topology is shown in Fig. 1. In this topology, inductors L_1 and L_2 are tightly coupled on the same ferrite core, and L_1 is the main inductor. S_1 and D_1 are the main power switches, like a conventional buck converter. D_2 is an additional diode. The theoretical current waveforms of L_1, L_2, and L_3 of the proposed converter at steady state are shown in Fig. 2. When S_1 is OFF, the converter comes into a free-wheeling stage. The branches of L_2 and L_3 will supply two flow channels for current free wheeling. Because L_3 is very small, the current of L_3 drops faster than that of L_1, and also reduces to zero before S_1 turns ON. It provides the ZCS condition for S_1. Due to snubber capacitor C_{r1}, S_1 can turn OFF under a ZVS condition. C_{p1} is the parasitic capacitance of the MOSFET S_1.

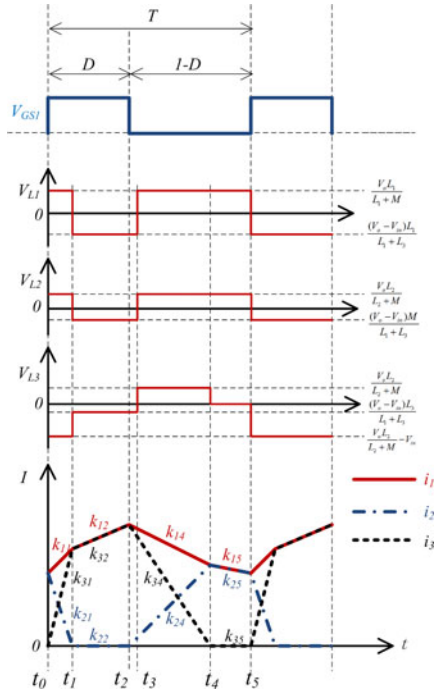

Fig. 2. Theoretical waveforms of i_1, i_2, i_3, and inductors' voltages in steady state.

B. Analyses of Operating Principles

Based on the waveforms of the inductor currents, one switching period is divided into five intervals, as shown in Fig. 2, and the equivalent circuits for each interval are given in Fig. 3, where the red solid arrows denote the actual current directions of each branch in each mode. In Fig. 2, k_{ij} indicates a slope of a different inductor current at a different mode, where i denotes the number of the inductor and j denotes the number of the different operating mode. The detailed theoretical analyses for each mode will be given as follows.

1) Mode I [$t_0 - t_1$, Fig. 3(a)]: Before t_0, the converter works at a current free-wheeling stage, and both i_3 and i_{s1} are equal to zero. At t_0, S_1 is triggered to conduct. Due to L_3, i_{s1} will increase slowly, so S_1 can turn ON under a ZCS condition. Then, i_3 and i_1 will increase, and i_2 will go down. Since L_3 is very small, the current-rising rate of L_3 is larger than that of L_1. At t_1, i_3 and i_1 are equal, and i_2 is zero. It means that D_2 turns OFF automatically, and this mode ends. Based on KVL and KCL, we can get

$$\begin{cases} i_1 = i_2 + i_3 \\ V_o - V_{L1} - V_{L2} = 0 \\ V_{L2} - V_{L3} - V_{\text{in}} = 0. \end{cases} \tag{1}$$

The voltage equations of inductors L_1, L_2, and L_3 can be expressed as follows:

$$\begin{cases} V_{L1} = -L_1 \dfrac{di_1}{dt} - M \dfrac{di_2}{dt} \\ V_{L2} = -L_2 \dfrac{di_2}{dt} - M \dfrac{di_1}{dt} \\ V_{L3} = -L_3 \dfrac{di_3}{dt} \end{cases} \tag{2}$$

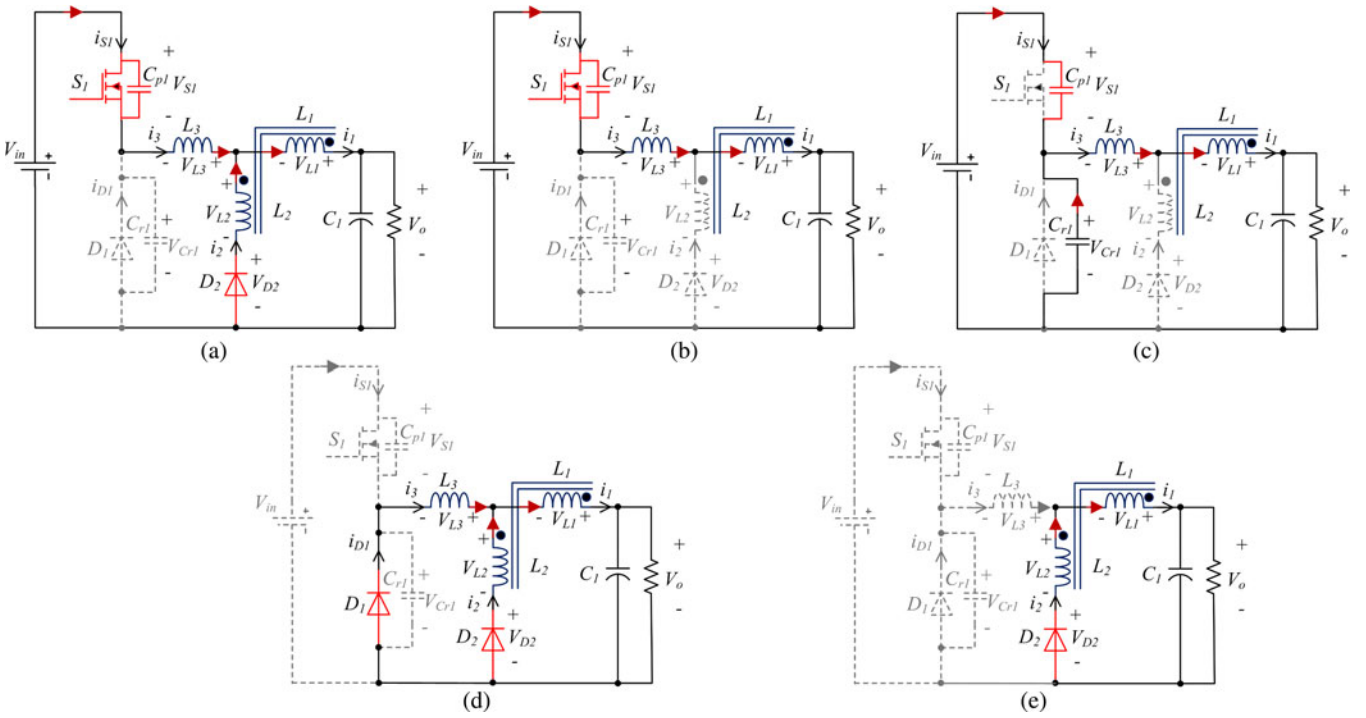

Fig. 3. Equivalent circuits for each operation mode of buck mode. (a) Mode 1, t_0–t_1. (b) Mode 2, t_1–t_2. (c) Mode 3, t_2–t_3. (d) Mode 4, t_3–t_4. (e) Mode 5, t_4–t_5.

where M is the mutual inductance and equal to $\sqrt{L_1 L_2}$.

Substituting (2) into (1), the slopes of i_1, i_2, and i_3 are obtained as follows:

$$k_{11} = \frac{di_1}{dt} = \frac{V_{\text{in}} L_2}{(L_2 + M)L_3} - \frac{V_o(L_3 + L_2)}{(L_1 + L_2 + 2M)L_3} \quad (3)$$

$$k_{21} = \frac{di_2}{dt} = -\frac{V_{\text{in}} L_1}{(L_1 + M)L_3} + \frac{V_o(M - L_3)}{(L_1 + L_2 + 2M)L_3} \quad (4)$$

$$k_{31} = \frac{di_3}{dt} = \frac{V_{\text{in}}}{L_3} - \frac{V_o L_2}{(L_2 + M)L_3}. \quad (5)$$

2) Mode 2 [$t_1 - t_2$, Fig. 3(b)]: After t_1, i_3 and i_1 are equal, and both increase linearly. In this mode, D_2 is always OFF, and the branch of L_2 does not work. At t_2, S_1 turns OFF, and this mode ends. It is similar to that of a conventional buck converter. The slopes of i_1, i_2, and i_3 are

$$k_{12} = k_{32} = \frac{di_1}{dt} = \frac{di_3}{dt} = \frac{V_{\text{in}} - V_o}{L_1 + L_3}; \quad k_{22} = 0. \quad (6)$$

3) Mode 3 [$t_2 - t_3$, Fig. 3(c)]: At t_2, S_1 turns OFF, and then a resonance occurs between inductors (L_1, L_3), parasitic capacitor C_{p1}, and snubber capacitors C_{r1}. C_{p1} is charged, and C_{r1} is discharged at the same time. When the voltage across C_{r1} reduces to zero, D_1 will conduct. This interval is very short, so it is assumed that the current in L_3 does not change in this mode. Because C_{p1} is very small, it can be neglected. Thus, the transition time T_{m1} can be obtained as follows:

$$T_{m1} = t_3 - \ t_2 = \frac{V_{\text{in}} C_{r1}}{I_{L3\max}}. \quad (7)$$

where $I_{L3\max}$, the value of i_3 at t_2, is positive and reaches a maximum in a switching cycle.

4) Mode 4 [$t_3 - t_4$, Fig. 3(d)]: When D_1 conducts, D_2 will conduct simultaneously. The condition that D_2 will conduct is shown in the following analyses. Firstly, it is assumed that D_2 could not turn ON. The numbers of the turns of L_1 and L_2 are n_1 and n_2, respectively, so

$$V_{L1} = V_o \times \frac{L_1}{L_1 + L_3}. \quad (8)$$

Then,

$$V_{L2} = \frac{n_2}{n_1} V_{L1} = \frac{n_2}{n_1} \times V_o \times \frac{L_1}{L_1 + L_3} = \sqrt{\frac{L_2}{L_1}} \times \frac{V_o L_1}{L_1 + L_3} = \frac{V_o M}{L_1 + L_3}. \quad (9)$$

From the KVL equation, we can get

$$V_o - V_{L1} - V_{L2} - V_{D2} = 0. \quad (10)$$

Substituting (8) and (9) into (10), we can obtain

$$V_{D2} = V_o \times \frac{L_3 - M}{L_1 + L_3}. \quad (11)$$

If D_2 conducts, V_{D2} must be less than zero, i.e., the next inequality must be met

$$L_3 < M. \quad (12)$$

After t_3, i_3 will decrease much faster than i_1 because L_3 is comparatively small. As long as i_3 reduces to zero, D_1 will turn OFF, and the condition of ZCS for S_1 is achieved. Then, this mode naturally ends. The current slopes of L_1, L_2, and L_3 can be derived as shown later.

After D_2 conducts, V_{D2} is equal to zero. Based on KVL and KCL, we can get

$$\begin{cases} i_1 = i_2 + i_3 \\ V_o - V_{L1} - V_{L3} = 0 \\ V_{L2} - V_{L3} = 0. \end{cases} \tag{13}$$

Substituting (2) into (13), the current slopes of the inductors are obtained as follows:

$$k_{14} = \frac{di_1}{dt} = -\frac{V_o(L_3 + L_2)}{(L_1 + L_2 + 2M)L_3} \tag{14}$$

$$k_{24} = \frac{di_2}{dt} = \frac{V_o(M - L_3)}{(L_1 + L_2 + 2M)L_3} \tag{15}$$

$$k_{34} = \frac{di_3}{dt} = -\frac{V_o(L_2 + M)}{(L_1 + L_2 + 2M)L_3}. \tag{16}$$

5) Mode 5 [$t_4 - t_5$, Fig. 3(e)]: At t_4, D_1 turns OFF, then a small resonance between L_3 and C_{r1} occurs, in which i_3 oscillates around zero and the amplitude is pretty small, so i_3 is supposed to zero in this mode. As shown in Fig. 3(e), the current just flows through L_1 and L_2, i.e., i_1 is equal to i_2. Therefore, the slopes of i_1, i_2, and i_3 can be easily obtained as follows:

$$k_{15} = \frac{di_1}{dt} = -\frac{V_o}{L_1 + L_2 + 2M} \tag{17}$$

$$k_{25} = \frac{di_2}{dt} = -\frac{V_o}{L_1 + L_2 + 2M} \tag{18}$$

$$k_{35} = 0. \tag{19}$$

III. Design of Main Circuits and Analyses of Simulation Results

A. Design of Main Circuits

To ensure that the proposed converter operates under the soft-switching condition, component parameters must be designed properly, especially the selections of the inductors (L_1, L_2, and L_3). From the analyses in Section II, the current of L_3 must be discontinuous to achieve soft-switching conditions. As the load increases, the duration that the current of L_3 remains zero will reduce to zero, and then L_3 will work at a continuous conduction mode (CCM), i.e., soft switching cannot be obtained. Therefore, the boundary conduction mode (BCM) between CCM and discontinuous conduction mode (DCM) can be used to calculate the parameters of main circuits. It can be assumed that the proposed converter would operate under BCM at a theoretic maximum load, which is more than the real maximum load. The theoretical waveforms of inductor currents at BCM are shown in Fig. 4. In this design, the theoretic maximum load is set to be 1.1 times the real maximum load.

In Fig. 4, it can be seen that mode 5 does not occur in BCM. Because the duration time of mode 3 is very short, it is not considered for calculating inductor parameters. One switching cycle can be divided into three intervals. Based on the slopes and variations of L_1, L_2, and L_3, some equations can be obtained as follows:

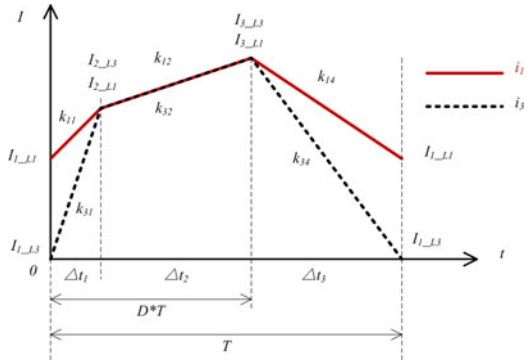

Fig. 4. Theoretical waveforms of inductor currents at BCM.

TABLE I
Related Target Specifications of the Proposed Converter

Parameters	Values
V_{in}	70 V
V_o	36 V
P_{output_max}	600 W
f_{sw}	50 kHz
T	20 μs
$I_{Load\_Max\_Real}$	16.7 A
$I_{Load\_Max\_Theoretic}$	18.4 A
I_{1_L1}	14.72 A
I_{2_L1}	17 A
I_{3_L1}	22.08 A
I_{1_L3}	0 A
I_{2_L3}	17 A
I_{3_L3}	22.08 A

follows:

$$\begin{cases} \Delta t_1 + \Delta t_2 + \Delta t_3 = T \\ k_{11} * \Delta t_1 = I_{2\_L1} - I_{1\_L1} \\ k_{31} * \Delta t_1 = I_{2\_L3} - I_{1\_L3} \\ k_{12} * \Delta t_2 = I_{3\_L1} - I_{2\_L1} \\ k_{14} * \Delta t_3 = I_{1\_L1} - I_{3\_L1} \\ k_{34} * \Delta t_3 = I_{1\_L3} - I_{3\_L3} \end{cases} \tag{20}$$

where $I_{1\_L1}, I_{2\_L1}, I_{3\_L1}, I_{1\_L3}, I_{2\_L3}$, and I_{3_L3} are attained by the theoretical maximum load average current, and the ripple coefficient of the inductor current. T is the time of one switching period. Then, $\Delta t_1, \Delta t_2, \Delta t_3, L_1, L_2$, and L_3 can be solved from (20), and the duty ratio D is equal to $(\Delta t_1 + \Delta t_2)/T$.

In this letter, a 600 W prototype is built, and the related target specifications are shown in Table I. Substituting these specifications into (20), the solved results are presented in Table II, where the basic equation in a buck converter, as $D = V_o/V_{\text{in}}$, is also meet in BCM.

TABLE II
SOLVED RESULTS OF INDUCTANCES AND DURATION TIMES

Parameters	Values
Δt_1	0.623 μs
Δt_2	9.66 μs
Δt_3	9.71 μs
L_1	62.3 μH
L_2	1.92 μH
L_3	2.37 μH
D	0.51

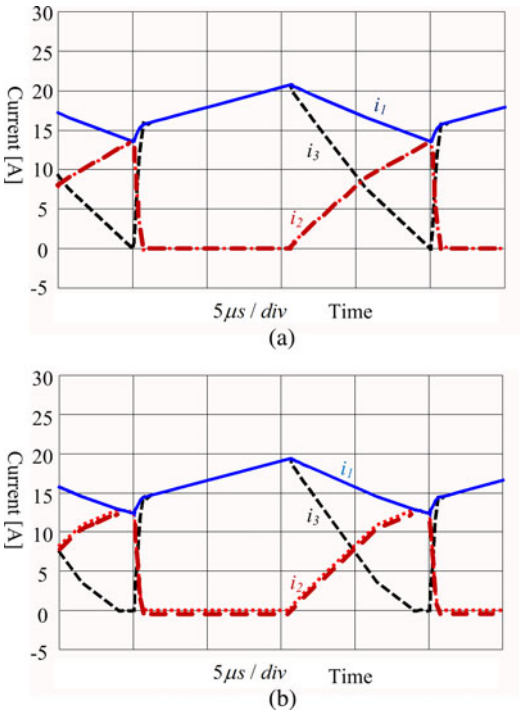

Fig. 5. Simulation waveforms of inductor currents. (a) Theoretical maximum load. (b) Real maximum load.

B. Analyses of Simulation Results

The simulation results are obtained from PSpice software. Using the parameters in Tables I and II, the simulation waveforms of i_1, i_2, and i_3 at the theoretical maximum load (18.4 A) and the real maximum load (16.7 A) are obtained, as shown in Fig. 5(a) and (b), respectively. In Fig. 5(a), it can be seen that inductor L_3 works under BCM, and mode 5 does not occur. In Fig. 5(b), i_3 remains zero in a short time, i.e., mode 5 exists here and ZCS turn on can be realized.

IV. EXPERIMENT RESULTS

According to the designed parameters in Section III, a prototype converter has been built to verify the aforementioned analyses. The photograph of the proposed converter prototype is shown in Fig. 6. For the power semiconductors, IRFP4232PBF by the International Rectifier is used for S_1, and 60EPU02PBF

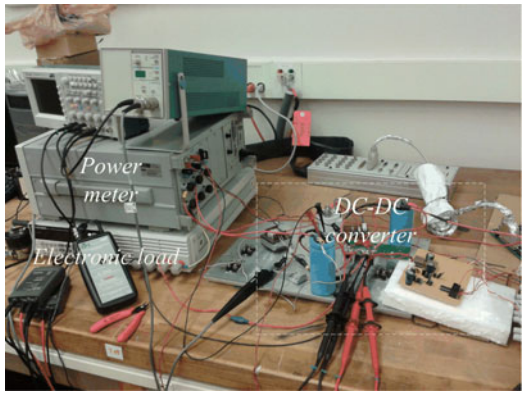

Fig. 6. Experimental setup of the proposed converter.

by Vishay Intertechnology is selected for D_1 and D_2. In addition, the magnetic powder cores of the inductors L_1, L_2, and L_3 are Kool Mu cores, which have low loss and relatively high saturation level (10 500 G). The part number of magnetic core of coupled L_1 and L_2 is 00K5530E060, 00K3007E060 is used for L_3, and both are produced by Magnetics. The inductances of the real inductors have some errors with the theoretically calculated values. In this converter, the turns of L_1, L_2, and L_3 are 18, 3, and 3, respectively. A 4700 pF polypropylene film capacitor is utilized for C_{r1}.

Switching waveforms of S_1 and the current waveform of L_3 are measured to validate soft-switching results. Efficiencies are also measured. However, i_{s1} is measured by an ac current probe, because the dc probe cannot be fixed on the MOSFET leg (package: TO-247). The real zero positions are marked in each figure.

A. Switching Waveforms

The switching waveforms of S_1 and current waveforms of L_3 are shown in Fig. 7, which is measured at the maximum output power 600 W. Fig. 7(a) shows the waveforms in a switching cycle, where the current of L_3 has been zero for a short time before S_1 is triggered ON.

The turn-on process of S_1 is shown in Fig. 7(b). After the gate trigger signal V_{GS1} is applied, current i_{s1} increases slowly. Therefore, ZCS turn on is achieved. In Fig. 7(c), the turn off of S_1 is presented. It can be seen that when the turn-off trigger signal is applied, i_{s1} decreases sharply to zero, and then V_{s1} increases to V_{in}. Hence, ZVS is also achieved in the turn-off process.

In Fig. 7(a) and (c), as the main switch is turning OFF, the claimed soft-switching condition (i.e., ZVS) is dominated by ringing. The ringing is caused by the stray inductance of the bus wires. When the main circuit is built in a PCB with a good layout, the stray inductance will decrease and the ringing will also be weakened.

B. Efficiency

The efficiency curve of the proposed converter is shown in Fig. 8, which demonstrates that high efficiency can be obtained

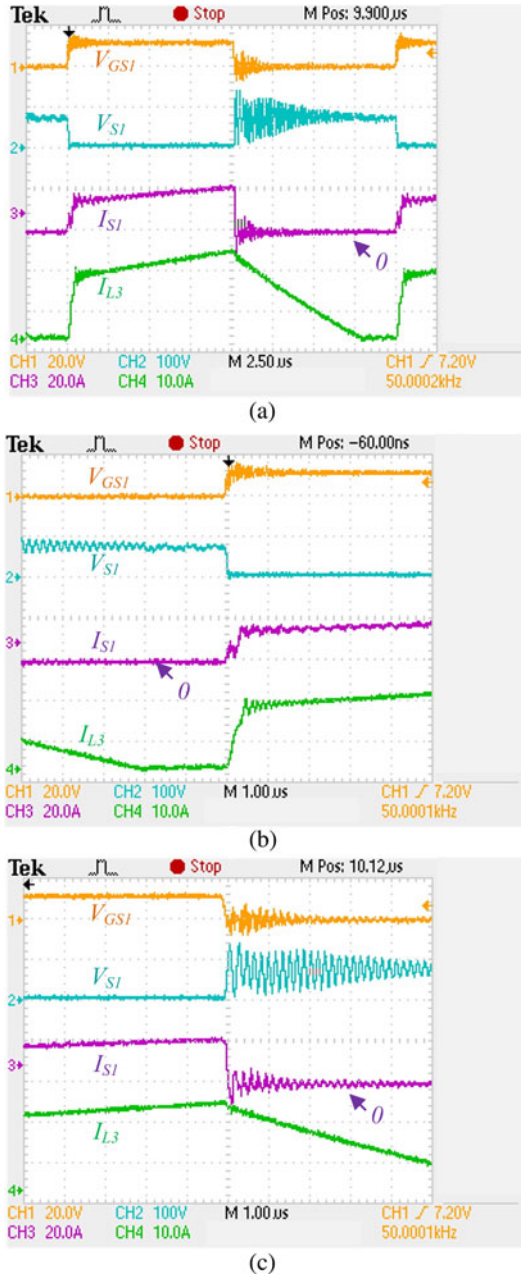

Fig. 7. Switching waveforms of S_1, and current waveform of L_3. (a) One switching cycle. (b) Turn-on process. (c) Turn-off process.

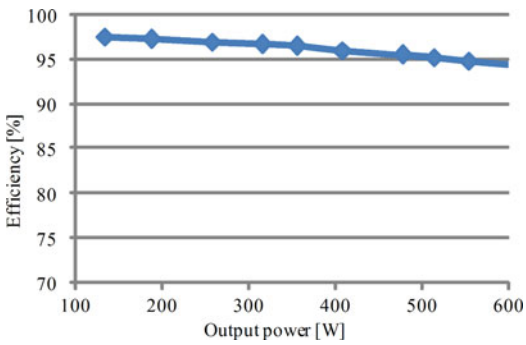

Fig. 8. Measured efficiency of the proposed converter.

in a wide range of load conditions. At the maximum load, the efficiency is 94.57%. When the load goes down, high efficiency can also be obtained. It is because L_3 usually works under DCM, and the conduction losses of the auxiliary circuits will decrease as the load reduces. The operating mode of auxiliary circuits is different from that of the converter in [18].

V. Conclusion

In this letter, a soft-switching buck converter with coupled inductor has been proposed. By making inductor L_3 to work under DCM, ZCS turn on and ZVS turn off for S_1 are achieved. The detailed theoretical analyses of the operating principle at steady state have also been given. The design methods of the main circuits are discussed. The prototype of the proposed buck converter was built, and the experiment results validated that soft switching of S_1 is achieved, and the related theoretical analyses are also verified. High efficiency can be obtained under both heavy load and light load conditions. Moreover, no auxiliary MOSFET is added in this topology, so the control method is as simple as that of a conventional buck converter.

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