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Modelling, design and optimisation of a battery charger for plug-in hybrid electric vehicles

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Abstract: A PowerPC-centred 110 VAC/2.5 kW full-bridge isolated battery charger was developed for the plug-in hybrid electric vehicle (PHEV). Genetic algorithm was adopted to optimise the system key parameters. Phase-shift-based operation modes were analysed in detail. The system-level safe operational area and other practical design considerations were discussed in detail. Experiments validated the design strategies. Finally, the optimisation of a fast PHEV charger was provided.

1 Introduction

Plug-in hybrid electric vehicles (PHEVs) can address the energy and environmental issues by using grid electricity to drive the vehicle in short driving distances, whereas the grid electricity can be generated from wide available renewable energy sources, such as hydro, wind and solar. From the technical aspect, PHEV is an optimised mix of various powertrain components, of which the electric charger is one of the most important components in a PHEV to charge the battery stack inside the vehicle.

State-of-the-art research and development motivates various charging circuits serving for different applications, where isolation is always demanded for safety and reliability. There are many feasible choices for the isolated unidirectional charging circuits. Flyback and forward converter are the typical examples. However, both these converters will induce high-voltage spikes owing to the existence of leakage inductance [1–4]. Therefore an auxiliary snubber circuit is needed especially at high-power operations. As an alternative, a half-bridge unidirectional DC–DC converter is a favourable choice for many applications [5, 6]. Different from the previous two topologies, this alternative magnetises the isolated transformer in both directions. Therefore the demagnetising circuit is no longer needed. Meanwhile the leakage inductance of the transformer is not injurious in the transient process, but necessary for energy transfer. The same principle applies to a full-bridge DC–DC converter [7, 8]. Compared with forward or flyback converters, the electrical pressure of semiconductors is reduced in half-bridge- and full-bridge-based chargers. Compared to half-bridge converters where only half of the secondary sets are conducting at any moment, a full-bridge converter utilises the transformer more efficiently. Although more semiconductors are needed in a full-bridge converter, soft-switching control can be easily implemented to increase system efficiency and reduce device pressure [9, 10]. The detailed comparison of different charger topologies is shown in Table 1.

In this paper, a full-bridge unidirectional topology is proposed. The system operation principle is described in Section 2. The design and optimisation is detailed in Section 3, including a genetic algorithm (GA) to optimise the circuitry parameters, a multi-layered bus bar to minimise stray inductance, and a system-level safe operational area (SOA) to guarantee the whole system to charge quickly and safely. Discussion on the high-power charger is presented in Section 4.

2 Overall system of the electric charger

Fig. 1 shows the general architecture of a PHEV charger. It consists of a front-end rectifier, a power factor correction (PFC) stage and an isolated DC–DC stage. PFC is important to correct the power factor and, more importantly, increase the power capability of the system for given components, as discussed in Section 4.

To simply the analysis, the PFC is neglected at first. Fig. 2 consists of a full-bridge unidirectional DC–DC converter and a rectifier, where the DC bus voltage on the primary side is V_1; the output voltage is V_2; the equivalent leakage inductance of the secondary side of the transformer is L_s; turns ratio is n, and switching frequency of the semiconductor switches is f_s. The input voltage of the system is 110 V AC from the electric grid.

During start-up of the circuit, S_1 is on and S_2 is off, the primary capacitor gets charged through R_1 and diode rectifier D_1–D_4. When the voltage of C_1 reaches 140 V ($0.9 \times 110 \times 1.414$), S_2 will be turned on and the pre-charge

Table 1 Comparison of different charging topologies

	Forward	Flyback	Half-bridge	Full-bridge
switch amount	smallest	smallest	middle	largest
peak current	average	average	depends on f_s and L_s	depends on f_s and L_s
inductor	largest	dispensable	dispensable	dispensable
voltage spikes	higher	highest	small	small
biased magnet	frequently	frequently	somewhat	seldom
soft switching	hard	hard	easy	easy
requirement for snubber	high	high	dispensable	dispensable
hard-switched loss	high	high	lower	lowest
application circumstances	low power	low power	high power	high power

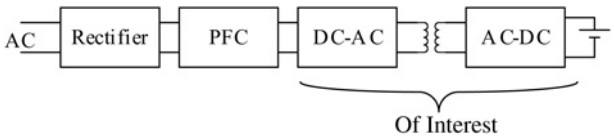

Fig. 1 *Basic PHEV charger architecture*

stage is complete. In this period, the inverter bridges remain idle and S_3 is off. After detecting start command with the right status of peripheral circuits, the PWM signals are generated to trigger MOSFETs T_1–T_4 to realise phase-shift control to charge C_2 through isolated transformer M and the secondary rectifier bridge D_5–D_8. Time sequence of the gate signals are shown in Figs. 3*a* and *b* where G_1–G_4 are the gate signals of T_1–T_4. In discontinuous mode, T_1 and T_2 are in zero current switching mode. When the voltage of C_2 reaches V_b, the battery voltage, S_3 will be turned on and the system enters into charging operation. In order to mitigate the influence of the high-frequency current ripple to the battery, a filtering inductor L_f is placed between C_2 and the batteries. Charging strategies will be detailed in the following sections.

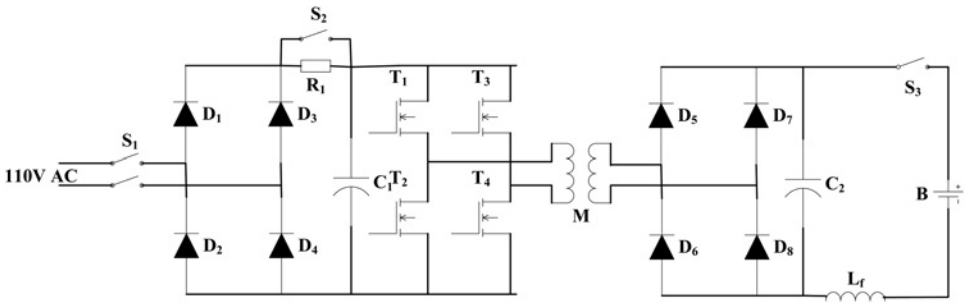

Fig. 2 *Schematics of the charger system*

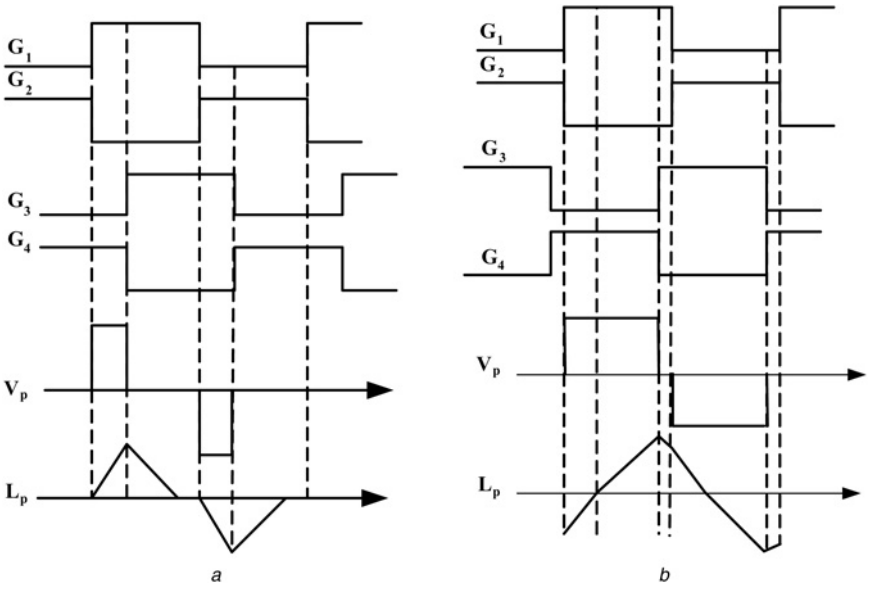

Fig. 3 *Operation modes of the charger*

a Discontinuous mode operation
b Continuous mode operation

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3 Design of key components

There are many constraints in the optimisation of the system. In general, optimisation should be based on the operational modes of the system. The key parameters, such as the peak current and maximum output power should be taken into account.

3.1 Operational modes of the system

In the discontinuous mode as Fig. 3*a*

$$I_{\max} = \frac{nD}{2L_s f_s}(nV_1 - V_2) \tag{1}$$

The averaged charging power is

$$P = \frac{nV_1 D^2}{4L_s f_s}(nV_1 - V_2) \tag{2}$$

Solve D in (2) and substitute it to (1), the maximum current can be derived

$$I_{\max} = \frac{\sqrt{nP(nV_1 - V_2)}}{\sqrt{nV_1 L_s f_s}} \tag{3}$$

When the phase shift increases, the operation will reach continuous mode as shown in Fig. 3*b*. The boundary of continuous mode and discontinuous mode is

$$D = \frac{V_2}{nV_1} < 1 \tag{4}$$

When the system is in the continuous modes, the peak current and output power is

$$I_{\max} = \frac{(nV_1 - V_2)}{4L_s f_s}\frac{(nV_1 D + V_2)}{V_1} \tag{5}$$

$$P = \frac{2D(nV_1)^2 - V_2^2 - (nV_1 D)^2}{8f_s L_s}\frac{V_2}{nV_1} \tag{6}$$

Especially when $D = 1$, the maximum power of the system can be delivered as

$$P = \frac{(nV_1 - V_2)(nV_1 + V_2)}{8f_s L_s}\frac{V_2}{nV_1} \tag{7}$$

and the maximum current of the MOSFETs is

$$I_{\max} = \frac{nV_1 - V_2}{4f_s L_s}\frac{nV_1 + V_2}{V_1} \tag{8}$$

Equations (3) and (5) show the peak current of the primary side as a comprehensive function of other parameters, for example, the leakage inductance of the transformer, the battery voltage and the switching frequency of the MOSFETs. From (8), the maximum current is decreasing when the battery voltage increases. In order to maximise the potential of the system, D should be increased to effectively charge the battery as long as the maximum current does not exceed the current capability of the semiconductors. The maximum output power in theory is different from that considering the current limits, as drawn later to detail the system SOA. In the prototype test set-up, the battery voltage ranges from 300 to 365 V.

In order to charge the battery with different current, a proportional-integral-derivative (PID) controller is used to modulate the phase-shift D and therefore realise the close-loop control of the charging current. The software flow chart is shown in Fig. 4. Here a constant current charging is adopted, which is followed by constant power charging and constant voltage charging.

3.2 Optimisation using the NSGA-II algorithm

The above analysis is focused on how to maximise the output power for given system parameters in the steady state. In real-world applications, high-power output is only one of the many concerns in the system design. An optimised DC–DC converter is required to have high efficiency, low cost, low-output voltage ripples, small-valued passive components (inductance or capacitance), low-current impact etc. At fixed output power, high efficiency and low electrical pressure of the semiconductors are mostly important. The charger for a PHEV consists of many components, and reasonable match of different parameters is important. Therefore how to reach the above goal is a typical multi-objective optimisation problem with some specific constraints, for example, maximum current peak of the semiconductors, baseline of the operating efficiency and maximum switching frequency.

In order to precisely calculate the system efficiency, a mathematic model was established that includes transformer, MOSFETs and diodes. Parameters of MOSFETs are listed in Table 2. Transformer parameters, n and L_s, need to be optimised.

The multi-objective optimisation problem can be expressed as (9), where η is the system efficiency. In order to achieve the desired power rating, two paralleled MOSFETs are used for each switch. Each MOSFET can handle 70 A at the ambient temperature of 25°C and 50 A at 75°C. Considering the possible imbalance of current distribution in the paralleled MOSFETs, the upper limit for the primary current peak $I_{\max}$ is set to 90 A. On the other hand, in order to utilise the MOSFETs efficiently, the lower boundary is set to 50 A when the output power is 2.5 kW.

$$\begin{array}{ll} \max & \eta \\ \min & I_{\max} \\ \text{subject to} & 1\,\text{kHz} \le f_s \le 200\,\text{kHz} \\ & 10\,\text{uH} \le L_s \le 100\,\text{uH} \\ & 50\,\text{A} < I_{\max} \le 90\,\text{A} \end{array} \tag{9}$$

Equation (9) shows that obtaining the optimal parameters in system is a typical multi-objective non-linear optimisation problem. The aim of multi-objective optimisation problems is to search the global optimal solution among multiple objective restraints. On the one hand, the conventional single-objective optimisation algorithm is hard to solve the multi-objective optimisation problems. One the other hand, since most of the multi-objective optimisation problems consist of a number of objectives, in reality none of the feasible solutions could offer optimal performance for all objectives. For example, in order to decrease peak current of the semiconductors, we can either increase the switching frequency or increase the leakage inductance. However, either of these methods will directly decrease the system efficiency and power capability. Therefore the mission of the

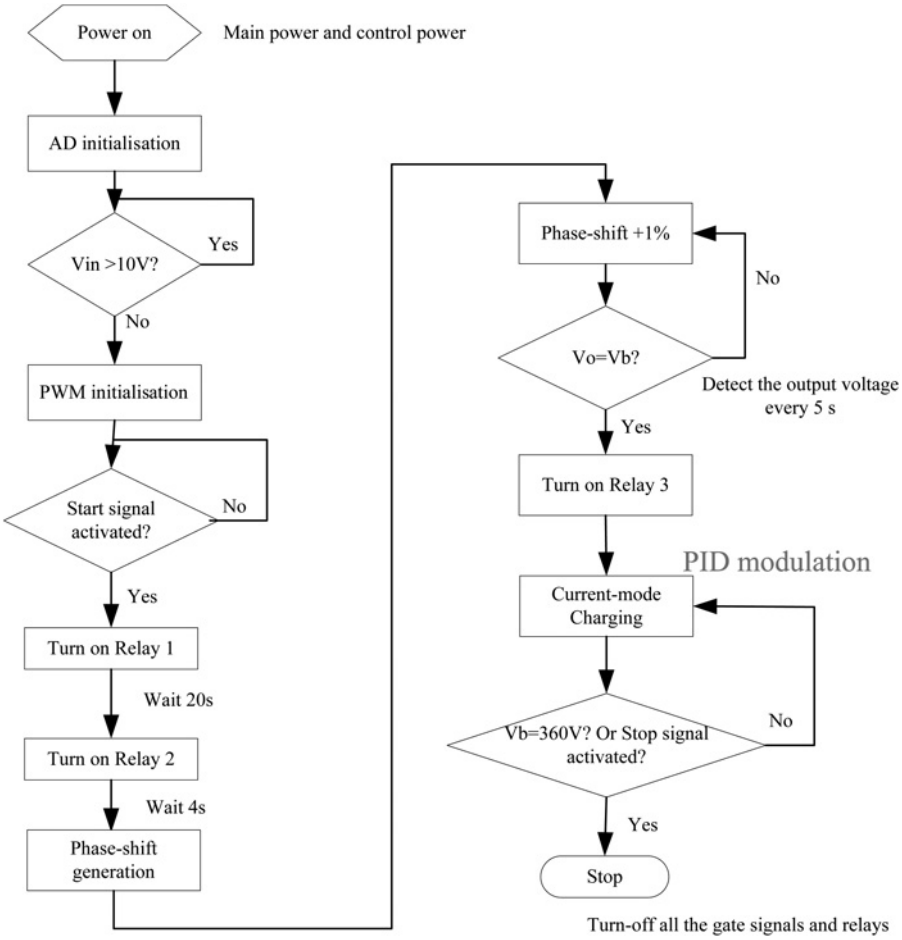

Fig. 4 *Starting process and close-loop current charging*

Table 2 Key parameters of MOSFETs

Name	Value
on-state resistance (R_{on})	65 mΩ
rise time (t_r)	27 ns
trailing time (t_f)	18 ns
reverse recovery time (t_{rr})	<200 ns

multi-objective optimisation is not to find out the results to be the best for a single constraint, but to find the solution with least objective conflict. GA is suitable for this type of optimisation problems.

GA is a natural selection- and genetics-based searching algorithm that can be applied to both linear and non-linear formulations. It randomises the mother generation, survives the fittest among the children generation and exchanges the information to form a search algorithm. In every generation, a new set of artificial creatures (strings) is created using the fittest of the old generation. Reproduction, crossover and mutation are the commonly used operations [11]. At present, in the engineering domain, non-dominated sorting genetic algorithm (NSGA-II) developed by Srinivas and Deb [11] is one of the most efficient evolutionary algorithms used to optimise a system. This paper will adopt this algorithm for the multi-objective optimisation.

The first step of this procedure is to initialise the size of population, generation number and number of objects and variables. Here decision variables are [n, f_s, L_s]. The individual is generated randomly within the boundary mentioned above. After initialisation, those individuals are regarded as the parent. Further effort is focused to generate the offspring of these parents by binary crossover operator, mutation, non-dominating sorting and the tournament selection. More details of this algorithm could be referred to [12, 13]. The computation steps for NSGA-II are shown in Fig. 5.

For the DC–DC converter in this paper, in order to fully maximise the system capability while minimising I_{max} and maximising efficiency of the system, some constraints are needed. The MOSFET current should not be too large to endanger the system or too low to waste the MOSFET capability. The switching frequency should not be too high to cause extra heat loss or too low to shade the MOSFET's advantages. This is used to set up the constraints in (9) for L_s, f_s, and I_{max}. The randomly selected parents and generated children are taken into the simulation model. Efficiency of the system can be calculated by the Simulink model and maximum current could also be obtained when the system reaches the steady-state operation. The optimising process of the specific parameters is shown in Fig. 6. The optimal solution for this DC–DC converter converging after ten-generation is $n = 2.98$, $L_s = 35.5$ μH, $f_s = 52.6$ kHz, efficiency = 88.3%, $I_{max} = 59.6$ A. In order to facilitate the design, the turn ratio is chosen to be 3.

3.3 DC bus bar design and transient energy flow

In order to minimise the stray inductance of the commutating loop, the MOSFETs and diodes are placed on the heat sink

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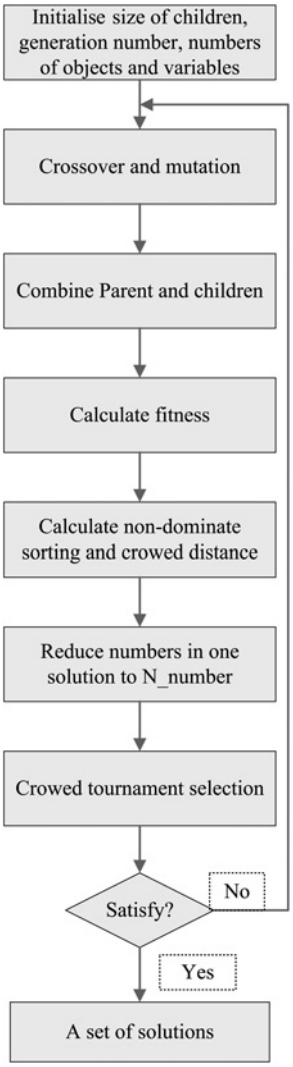

Fig. 5 *Flow chart of the GA*

closely to each other, and the bus bars are laid out on a single printed circuit board (PCB) board, which makes the largest stray inductance of the commutating loops only 60 nH, acquired through finite-element analysis. Experimental results show that the trailing edge of MOSFETs lasts 100 ns in this system (increased R_{GS} to 5 Ω). Therefore the calculated maximum voltage peak when the current in each MOSFET reaches 50 A is

$$\Delta V = L\frac{I}{t_f} = 30(\mathrm{V}) \tag{10}$$

Therefore the DC bus voltage plus the voltage spike is far below the voltage capability of the MOSFET, 500 V. This shows the huge advantages of multi-layered DC-bus bar. In practice, the influence of the stray inductance of the commutating loop can be minimised because of low stray inductance.

3.4 System-level SOA

Owing to the low stray inductance in the commutating loop and low DC-bus voltage, the possibility of over-voltage across the MOSFETs could be neglected. Current impact comes to be the primary concern. The direct object of the charger is the battery. Assume the MOSFETs can handle large current, then the maximum output power of the system determined by (7) can be plotted in Fig. 7 as C_1 and C_3 when the battery voltage ranges from 20 to 365 V. Consider the voltage fluctuation on the DC-bus, C_1 and C_3 are the cases when $V_1 = 140$ and 150 V, respectively.

However, with the decrease in battery voltage V_2, the risk of the impact of large current to the MOSFETs emerges according to (8) if the device is operated under high-power output. Decreasing the charging power will help ease the current impact but increase charging time. Meanwhile to charge the battery with trickling current at low voltage can also be helpful to prevent potential damage to the battery [14]. If the charger is regarded as a black box, in the medium voltage range the output power should be maximised as long as the MOSFET voltage and current are not beyond its capability. In this device, the maximum output power of the system is shown as C_2 and C_4 with $V_{dc} = 140$ and 150 V, respectively.

With the above-optimised parameters, the maximum power this device can generate is recommended as the shadowed region shown in Fig. 7*a*. When battery voltage equals 310 V, the maximum output power will reach 4.5 kW. Therefore the recommended charging curve is plotted in Fig. 7*b*, where the horizontal axis is the battery voltage and the vertical axis is the battery charging current. Any point located inside the shadowed region will make sure the system is reliable. For simplicity, the control could also be adjusted as the bold arrow lines, that is, within each voltage segment the battery is charged with a constant current value.

In most cases, the SOA of a power electronic system targets the semiconductor devices [15]. It includes the recommended voltage and current of semiconductors, however seldom people consider the variation caused by the load, stray parameters and control algorithms. This is the difference between device-level SOA and system-level SOA. Hua *et al.* [16] firstly proposed the concept of system-level SOA of a three-level inverter. Fig. 7*b* is regarded as the extension of this concept, which comprehensively combined the consideration of DC-bus voltage and its fluctuation, maximum voltage/current capability of the MOSFETs, the influence of the stray inductance (although here its influence has been depressed by the bus-bar design), and the load variation. It will directly impact the control, design and application of the system.

In Fig. 8, the influence of the different leakage inductance is shown. When L_s increases, the capability of charging battery at a low-voltage range is enhanced. However, it will be weakened in the high-voltage range.

3.5 Test platform and experimental validation

The charger was built and tested with lithium batteries. The batteries consist of 25 battery modules rated at 4 Ah. Each module consists of four rows in series and 32 standard lithium battery cells in parallel per row. The batteries are made with lithium iron phosphate chemistry. Each cell is 18 mm in diameter, 65 mm height, with 1.35 Ah capacity and 3.2 V nominal voltage. The cell voltage reaches 3.65 V when fully charged. Recommended continuous charging current is 1/2 C, or 0.67 A/cell; or 22 A/pack.

Fig. 9*a* shows the output voltage of the H-bridge with phase shift changing to 75%. The battery voltage is 337 V, close to the rated 365 V. The input power is 2.1 kW and the output power is 1.86 kW. Therefore the efficiency is 88.7%, which is very close to the predicted data by the generic algorithms.

The voltage and current waveforms are shown in Fig. 10, where V_{ds} is the voltage drop across the single MOSFET,

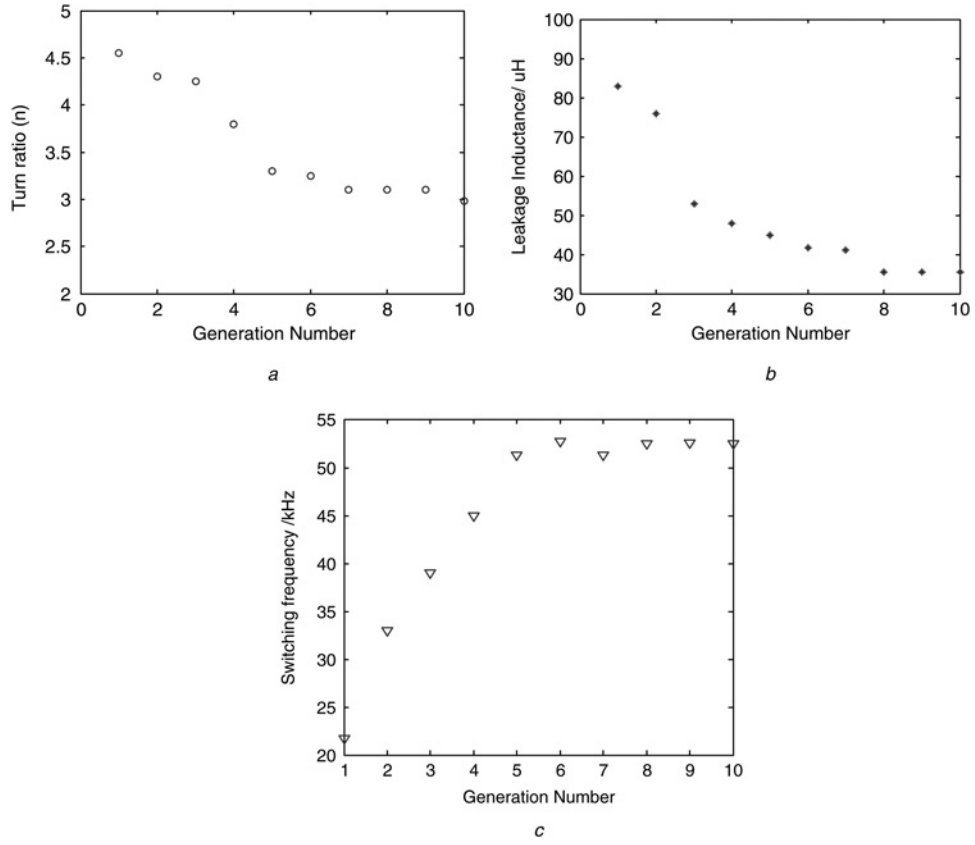

Fig. 6 *Results of the optimisation procedure*

a Optimisation of the turn ratio
b Optimisation of the leakage inductance
c Optimisation of the switching frequency

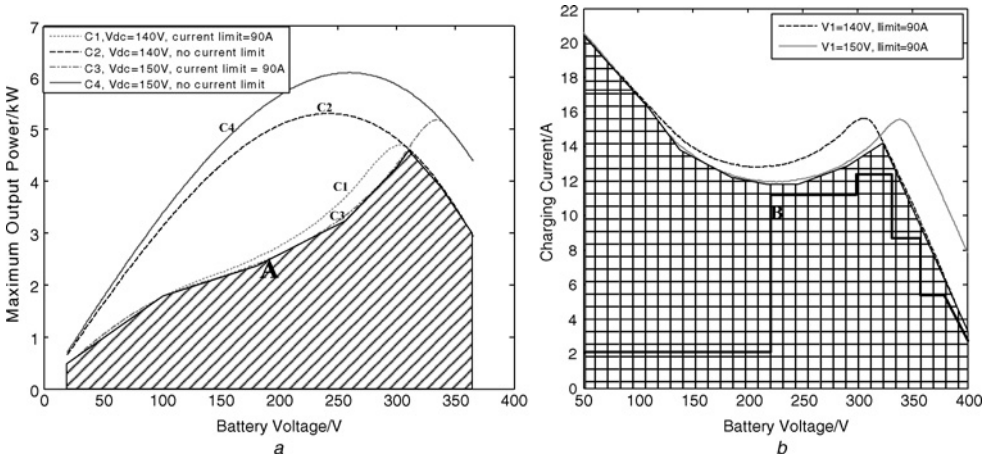

Fig. 7 *Analysis of power capability at different load conditions*

a Power capability of the system
b Quasi-dynamic system-level SOA

V_p is the primary voltage of the transformer and I_p is the primary current. When $V_{dc} = 150$ V DC, the voltage spike on the single MOSFET is negligible as shown in Fig. 9*b*. The small voltage spike across the MOSFET attributes to the compact DC-bus layout in the prototype, where the multi-layer-structured DC bus is adopted. The leakage inductance of the transformer does not induce any voltage peak. It is worth pointing out that the voltage distortion in Fig. 9 is caused by the dead-band effect where the primary current of the MOSFET is discontinuous.

3.6 Design of a high-power charger

It must be pointed out that the above optimal parameters are all obtained when the DC-bus voltage is ~150 V. The multi-objective problem shown in (9) will have different solutions when the constraints change. For example, when the DC bus voltage is boosted to 200 V DC, the MOSFET current is expected to decrease for the same output power, as shown in Fig. 10 where the current peak of the MOSFETs is <20 A at the rated power (2.5 kW).

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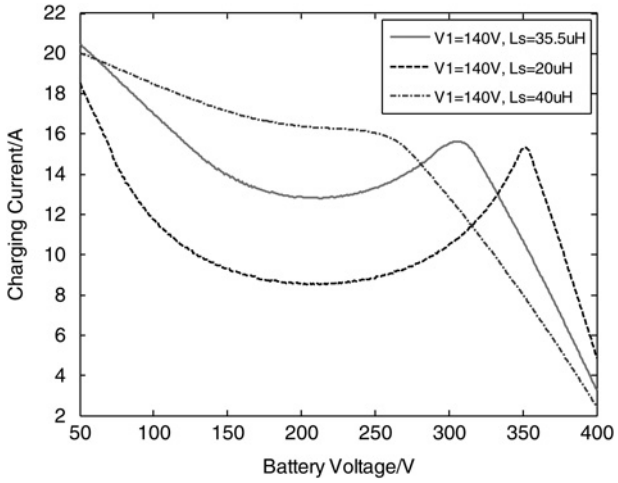
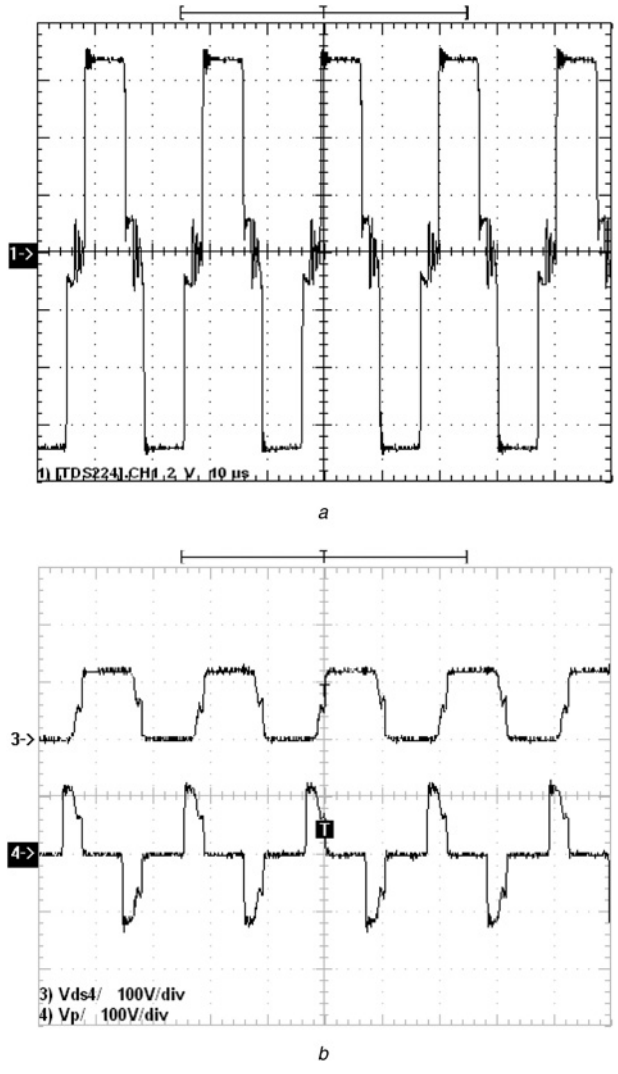


Fig. 8 *Influence of leakage inductance on charging power*



a

b

Fig. 9 *Output voltage waveforms of the charger*

a Output voltage of the H-bridge at rated voltage and heavy load (experimental results)
b V_{ds} and V_p (experimental results)

Experimental results show that the circuit could handle 2.5 kW output with 150 V DC bus voltage. However, it is very hard to reach 5 kW because of the high current. In some applications, when a higher charging power capability is required, the input source is 220 V AC instead of 110 V AC; 220 V AC transmission line will undertake higher power flow than 110 V AC, and it will increase the DC bus voltage and decrease the DC-bus current at the same output power. Fig. 11 shows the comparison of the switch currents at the same output power (5 kW) with different DC-bus voltage.

Furthermore, in order to improve the quality of the input electricity, for the 5 kW power charger, a PFC is used to

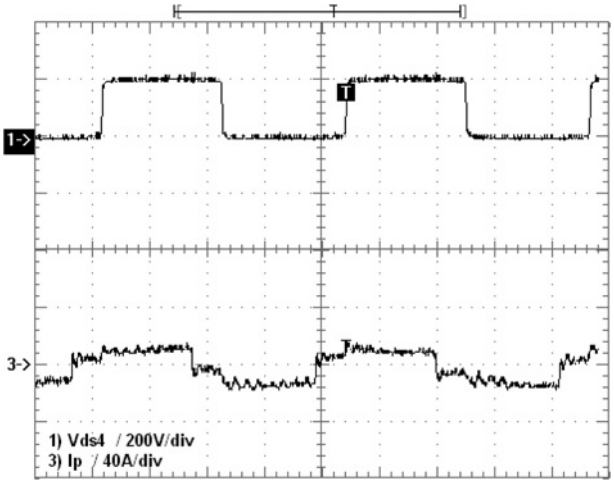


Fig. 10 *V_{ds} and I_p when $P_{out} = 2$ kW*

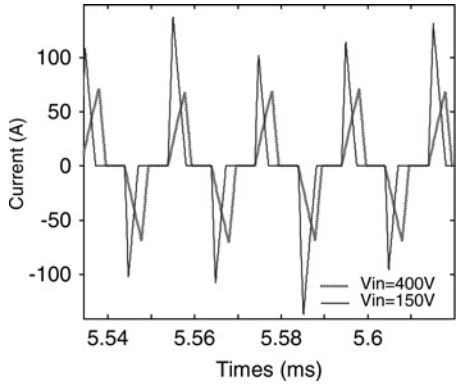


Fig. 11 *Comparison of switch current*

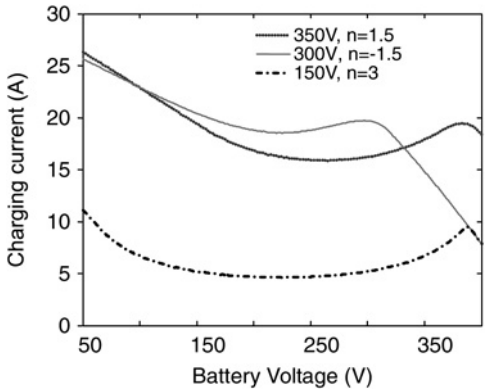


Fig. 12 *Maximum charging current under different DC-bus voltage (using PFC and single MOSFET module)*

correct the power factor and boost the DC-bus voltage to a higher value. In that case, the above optimisation procedure should be rerun. Since 400 V is too close to the break-down voltage of the MOSFET, the DC-bus voltage at controlled at 350 V. The optimisation for a 5 kW charger is: $n = 1.5$, $f_s = 50$ kHz, $L_s = 20$ uH and $I_{max} = 60$ A. If we set the upper boundary of the peak current to 70 A, the maximum charging current at different battery voltage is illustrated in Fig. 12. It is shown that with the DC-bus voltage changing, the redesigned system has much higher output capability than the older version.

4 Conclusion

This paper detailed the specific steps to model, design and optimise a charger for PHEVs. Generic algorithms are adopted to obtain the optimal value of the passive components. Its feasibility has been proven by many previous literatures in the vehicle domain [17–19]. In the hardware design, the bus bar is laid out to minimise the influence of stray inductance. After the combination of all above factors, the system-level SOA is modified to fit the charging curve, which helps maximise the system output capability. Some preliminary results are given for the optimisation of a higher-power charger. Additional effort is centred on the charging algorithm development that helps extend battery life and maximise the battery capacity.

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