

A Delta-Structured Switched-Capacitor Equalizer for Series-Connected Battery Strings

Yunlong Shang , *Member, IEEE*, Chenghui Zhang , *Senior Member, IEEE*, Naxin Cui , *Member, IEEE*, and Chunting Chris Mi , *Fellow, IEEE*

Abstract—The classical switched-capacitor (SC) equalizer is widely used in battery management systems because of the accurate balancing and ease of implementation. However, it only achieves the adjacent cell-to-cell equalization, and its balancing speed and efficiency become extremely low for multicell series-connected battery strings. Therefore, a delta-structured switched-capacitor equalizer is introduced to achieve a high-speed and high-efficiency any-cells-to-any-cells (AC2AC) equalization at arbitrary imbalanced status for any number of cells. The slow switching limit and fast switching limit impedances of the proposed equalizer are developed to provide a theoretical guidance for the optimized design of the SC equalizers. A prototype for four battery cells was built, and a comparison with existing equalizers was presented. Experimental and comparative results show that the proposed solution exhibits an automatic AC2AC balancing with high reliability and strong robustness. The measured balancing efficiency is up to 94.5%.

Index Terms—Automatic equalizers, battery management systems (BMS), electric vehicles (EVs), switched capacitors (SCs).

I. INTRODUCTION

LITHIUM-ION batteries are widely used in numerous high-power applications such as energy storage systems and electric vehicles (EVs) [1], [2]. In order to achieve a high output voltage, a large number of lithium-ion battery cells are connected in series [3]. However, due to the tolerance in manufacturing, the battery cells may not have the same cell internal resistance, self-discharge rate, and capacity [4]. These differences cause the cell voltage inconformity in the charging or discharging processes of the battery pack. All cells in the bat-

tery string should be operated within the allowed voltage range, e.g., 2–365 V for LiFePO₄ batteries [5]. When an arbitrary cell in the battery pack is outside the allowed range, the operation for the battery pack must be terminated, which reduces tremendously the storage capacity of the battery pack [5]. Therefore, battery equalizers are needed to balance the cell voltages to maximize the available capacity of the battery stack. In addition, the cost of battery packs can be reduced dramatically, because the requirements in cell consistency can be loosened when battery equalizers are introduced.

Numerous active balancing methods have been reported in [5]–[32]. According to the control strategies, battery equalizers can be divided into four categories, including the voltage-based [5], state of charge (SoC)-based [6], pack capacity based [7], and automatic balancing methods. SoC-based and pack capacity based equalization solutions [7] can maximize theoretically the available capacity of the battery string, but require accurate SoC and capacity estimation for each cell, leading to a great amount of calculation and low balancing accuracy, which are very difficult to be implemented in EVs. Voltage-based balancing methods [5] with the intention of the same cell voltage can be easily implemented. However, this method needs to judge the highest and lowest cell voltages and find the positions of the highest and lowest voltage cells, leading to a complex control for a multicell series-connected battery string. Moreover, this method tends to cause over-equalization or under-equalization for a battery string due to the imbalanced internal resistances of cells. Particularly, in case of cell voltage measuring failure, the voltage-based equalization will run out, thus resulting in a low reliability. In contrast, the automatic balancing is executed based on the natural property of the equalizer with an open-loop control. In the other words, energy flows automatically from more-charged cells to less-charged ones without the requirement of any cell monitoring devices. The balancing current is proportional to the voltage difference, avoiding the over-equalization or under-equalization. Although the automatic balancing method does not represent the ultimate target of balancing, it has outstanding advantages of simple control, accurate balancing, high reliability, and strong robustness. It is worth mentioning that it is unnecessary to pursue a large balancing current even for a large capacity battery string. On the one hand, the inconsistency of the battery string develops very slowly and there is enough time to balance imbalanced cells with a small balancing current. In addition, too large balancing current/power will lead to a large size, high cost, and high energy loss.

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Y. Shang is with the School of Control Science and Engineering, Shandong University, Jinan 250061, China, and also with the Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA 92182 USA (e-mail: shangyunlong@mail.sdsu.edu.cn).

C. Zhang and N. Cui are with the School of Control Science and Engineering, Shandong University, Jinan 250061, China (e-mail: zchui@sdsu.edu.cn; cuiinx@sdsu.edu.cn).

C. C. Mi is with the Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA 92182 USA (e-mail: cmi@sdsu.edu).

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According to energy flows, battery equalizers can be further divided into six categories: cell-to-resistor (C2R) [8], adjacent cell-to-cell (AC2C) [9]–[17], direct cell-to-cell (DC2C) [18]–[20], cell-to-pack (C2P) [21], [22], pack-to-cell (P2C) [23]–[25], and any-cells-to-any-cells (AC2AC) [26]–[32] methods. The C2R employs a resistor for each cell to consume excess energy from the more-charged cells, which has the clear advantages of small size, low cost, and easy implementation, but has the serious problems of energy dissipation and heat management. The AC2C method only transfers energy from one cell to the adjacent one, leading to a serious low balancing speed and efficiency for a multicell battery string. However, it has some obvious advantages, e.g., simple structure, low cost, small size, low voltage stress on components, and easy implementation. Compared with the AC2C method, the DC2C method can directly transfer energy between arbitrary two cells regardless of their positions in the battery string. Unfortunately, the DC2C method only balances simultaneously the selected two cells, resulting in a low balancing speed for numbers of cells. The C2P and P2C methods can transfer energy between the individual cell and the whole battery pack, achieving an improved balancing speed. However, the step-up or step-down conversion ratio of the equalizer is extremely high or low for a large battery string, resulting in a low conversion efficiency and high voltage stress on switches. Compared with the above-mentioned methods that only obtain the “time-shared” balancing for cells, the AC2AC methods can simultaneously transfer energy from all the higher voltage cells to all the lower voltage cells, leading to a higher balancing speed and efficiency.

Evzelman *et al.* [26] proposed a distributed bypass balancing architecture, which achieves the continuous AC2AC equalization for all cells, leading to a fast balancing speed. Particularly, this equalizer can achieve the SoC and capacity-based equalization, making full use of the energy of the battery string. Another highlight of this topology is the easy modularity. Li *et al.* [29] proposed a simple structure of battery equalizer based on forward conversion. Without the need of cell monitoring circuits, energy can be automatically delivered from arbitrary more-charged cells to arbitrary less-charged ones. However, the balancing effect is very poor, which depends heavily on the consistency of the multiple windings, including the magnetizing inductance, leakage inductance, equivalent resistance, etc. By comparison, capacitor-based solutions can achieve accurate voltage balancing independent of the capacitor consistency. For example, the classical switched-capacitor equalizer (CSCE) [9] only needs one capacitor for every adjacent two cells and is the simplest one with a smaller size and lower cost. However, it only achieves the AC2C equalization, leading to a seriously low balancing speed and efficiency for a multicell battery string. The double-tiered of SC equalizer (DTSCE) [10] employs an additional capacitor to bridge the first-tiered capacitors, which can directly exchange energy between the top and bottom cells, to some extent, improving the balancing speed and efficiency. It is worth to mention that Ye *et al.* [31] developed a great improved SC equalizer, i.e., the star-structured SC equalizer (SSSCE), to achieve a high balancing speed and efficiency independent of the initial imbalanced statuses of cell voltages. However, the

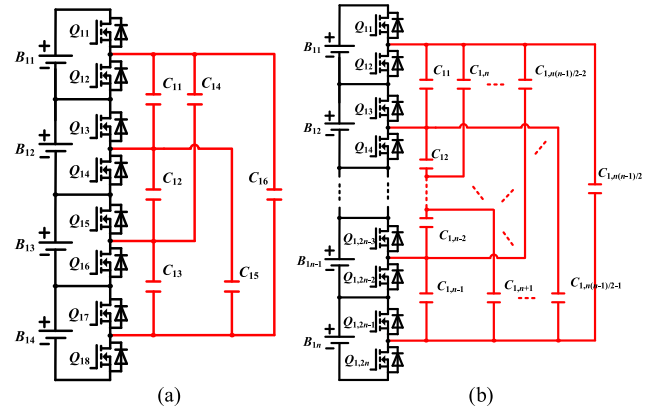


Fig. 1. Proposed DSSCEs. (a) For a four-cell battery string. (b) For an n -cell battery string.

energy from the source cell must go through two capacitors before arriving at the target cells, leading to a decreased balancing current and increased energy loss. Therefore, each capacitor should have twice the capacitance as the CSCE [9] to achieve the same balancing current/speed, which contributes to a large size and high cost.

To solve these problems, this paper introduces a delta-structured switched-capacitor equalizer (DSSCE) to achieve fast-speed and high-efficiency AC2AC equalization independent of the imbalanced statuses of battery strings without significant changes in the size, cost, and reliability.

II. PROPOSED EQUALIZER

A. Configuration of the Proposed Equalizer

Fig. 1(a) shows the schematic diagram of the proposed DSSCE for a four-cell battery string [33]. In this configuration, two series-connected MOSFETs are needed for each cell with one capacitor for every adjacent two cells. Except for this classical design [9], additional two-tiered capacitors are added to be parallel with the first-tiered capacitors to ensure one capacitor being set for any two cells, materializing the delta-structured switched capacitors (DSSCs). Like the SSSCE [31], this structure also offers all the direct balancing paths between arbitrary two cells in a battery string, achieving an effective AC2AC balancing independent of the initial imbalanced status of the battery string. Moreover, in one switching cycle, the balancing energy only travels through one capacitor, improving the balancing efficiency and capacity. Particularly, the precise voltage equalization could be achieved without any requirements for the capacitance matching. Fig. 1(b) further presents the proposed equalizer with $n - 1$ -tiered capacitors applied to an n -cell series-connected battery string.

B. Operation Principles

Similar to the CSCE [9], the proposed DSSCE is driven by two opposite-state pulsewidth modulation signals and has two steady phases in one switching period. These two working phases are operated alternatively with a high frequency and energy is automatically exchanged between arbitrary higher voltage battery

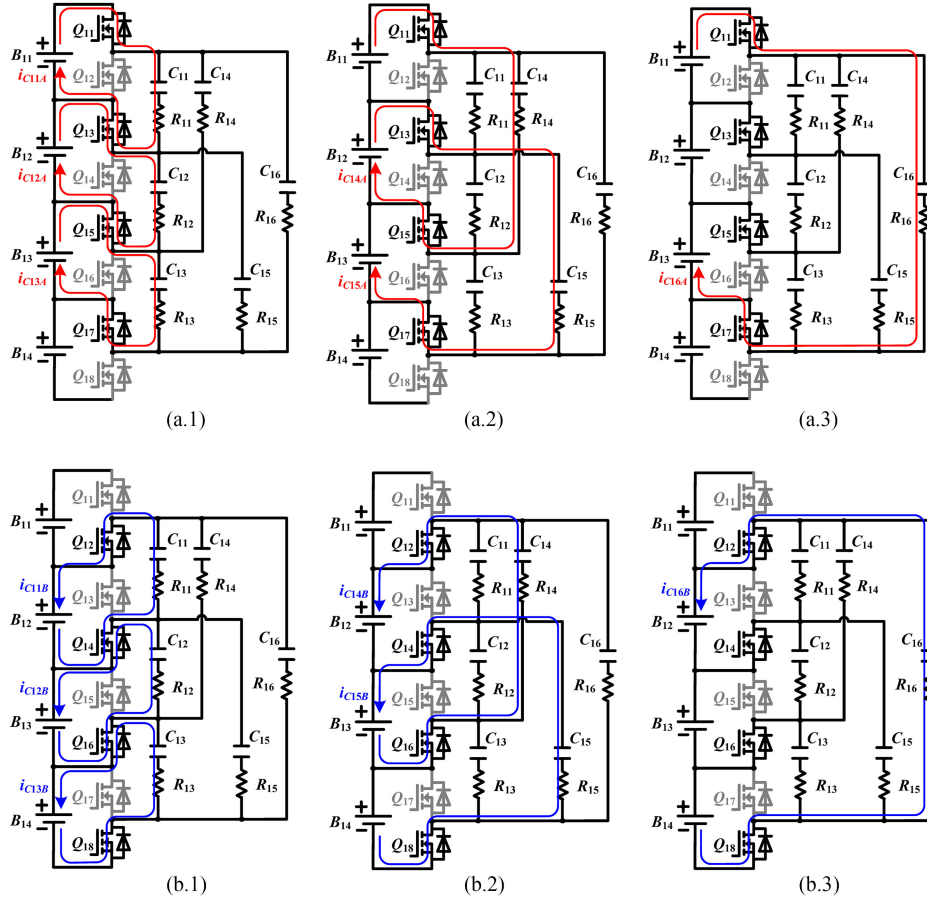


Fig. 2. Operating phases of the proposed DSSCE at $V_{B11} > V_{B12} > V_{B13} > V_{B14}$. (a.1)–(a.3) Phase A. (b.1)–(b.3) Phase B.

cells and arbitrary lower ones. Fig. 2 shows the operating phases under the assumption of $V_{B11} > V_{B12} > V_{B13} > V_{B14}$.

Phase A [t_0 – t_1 , Fig. 2(a)]: The DSSCs are connected in parallel with the corresponding upper cells B_{11} – B_{13} through the odd switches Q_{11} , Q_{13} , Q_{15} , and Q_{17} . During this phase, the redundant energy of B_{11} – B_{13} is transferred to the DSSCs with six balancing paths, i.e., i_{11A} – i_{16A} .

Phase B [t_1 – t_2 , Fig. 2(b)]: The DSSCs are connected in parallel with the corresponding lower cells (B_{12} – B_{14}) through the even switches Q_{12} , Q_{14} , Q_{16} , and Q_{18} . During this phase, the energy stored in the DSSCs is transferred to B_{12} – B_{14} with six balancing paths, i.e., i_{11B} – i_{16B} .

It can be observed that the proposed equalizer can directly transfer energy between arbitrary two imbalanced cells in the battery string without the requirement of cell monitoring circuits and closed-loop controllers. Moreover, the balancing among cells is synchronous.

C. Switching Limit Impedance Analysis

The slow switching limit (SSL) and fast switching limit (FSL) impedances [34] are developed to provide a reference to choose the switching frequency. It is assumed that the voltage gaps among cells meet $V_{B11} = V_{B12} + \Delta V = V_{B13} + 2\Delta V = V_{B14} + 3\Delta V$. Based on Kirchhoff's current

law (KCL), the average balancing currents flowing through the capacitors and cells during phases A and B can be expressed, respectively, as

$$\begin{cases} I_{C11A} = I_{C12A} = I_{C13A} = I_r \\ I_{C14A} = I_{C15A} = 2I_r \\ I_{C16A} = 3I_r \\ I_{B11A} = I_{C11A} + I_{C14A} + I_{C16A} = 6I_r \\ I_{B12A} = I_{C12A} + I_{C14A} + I_{C15A} + I_{C16A} = 8I_r \\ I_{B13A} = I_{C13A} + I_{C15A} + I_{C16A} = 6I_r \end{cases} \quad (1)$$

$$\begin{cases} I_{C11B} = I_{C12B} = I_{C13B} = -I_r \\ I_{C14B} = I_{C15B} = -2I_r \\ I_{C16B} = -3I_r \\ I_{B12B} = I_{C11B} + I_{C14B} + I_{C16B} = -6I_r \\ I_{B13B} = I_{C12B} + I_{C14B} + I_{C15B} + I_{C16B} = -8I_r \\ I_{B14B} = I_{C13B} + I_{C15B} + I_{C16B} = -6I_r \end{cases} \quad (2)$$

where I_r is the reference balancing current.

According to (1) and (2), it can be seen that cells B_{12} , B_{13} are first discharged during phase A and then are charged during phase B. In order to ensure that each cell is only charged or discharged during one switching phase, two virtual capacitors C_{17} and C_{18} with the same capacitance as the regular capacitors

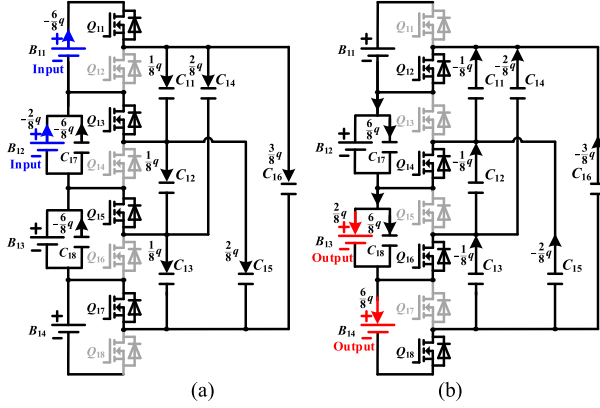


Fig. 3. Charge flows of the proposed equalizer. (a) Phase A. (b) Phase B.

C_{11} – C_{16} are employed to be connected in parallel with B_{12} and B_{13} , respectively. Under these conditions, as shown in Fig. 3, B_{11} , B_{12} only serve as the outputs during phase A, and B_{13} , B_{14} only serve as the inputs during phase B. According to (1) and (2), during one switching period, the total input charge q_{in} flowing out of B_{11} and B_{12} and the total output charge q_{out} flowing into B_{13} and B_{14} can be given by

$$q_{in} = q_{out} = 8I_r \cdot T \quad (3)$$

where T is the switching period. Based on (1) and (2), as shown in Fig. 3(a) and (b), the charges flowing through capacitors during phases A and B can be deduced, respectively, as

$$\begin{aligned} \mathbf{a}^A &= [a_{out}^A \ a_{C11}^A \ a_{C12}^A \ a_{C13}^A \ a_{C14}^A \ a_{C15}^A \ a_{C16}^A \\ &\quad \times a_{C17}^A \ a_{C18}^A \ a_{in}^A]^T \\ &= \begin{bmatrix} 0 & \frac{1}{8} & \frac{1}{8} & \frac{1}{8} & \frac{2}{8} & \frac{2}{8} & \frac{3}{8} & -\frac{6}{8} & -\frac{6}{8} & -1 \end{bmatrix}^T, \end{aligned} \quad (4)$$

$$\begin{aligned} \mathbf{a}^B &= [a_{out}^B \ a_{C11}^B \ a_{C12}^B \ a_{C13}^B \ a_{C14}^B \ a_{C15}^B \ a_{C16}^B \\ &\quad \times a_{C17}^B \ a_{C18}^B \ a_{in}^B]^T \\ &= \begin{bmatrix} 1 & -\frac{1}{8} & -\frac{1}{8} & -\frac{1}{8} & -\frac{2}{8} & -\frac{2}{8} & -\frac{3}{8} & \frac{6}{8} & \frac{6}{8} & 0 \end{bmatrix}^T \end{aligned} \quad (5)$$

where a_{C1i}^A and a_{C1i}^B are, respectively, the ratios of the charges transferred in each capacitor during phase A and phase B to the total output charge q_{out} during one switching period. a_{in}^A and a_{in}^B are, respectively, the ratios of the input charges during phase A and phase B to the total input charge q_{in} during one switching period. a_{out}^A and a_{out}^B are, respectively, the ratios of the output charges during phase A and phase B to the total output charge q_{out} during one switching period. It is specified that the ratio is positive when the charge flows into the element, otherwise is negative.

At low switching frequencies, the SSL impedance is mainly dependent on the capacitor losses [34]. Based on KCL, Kirchhoff's voltage law, and Tellegen's theorem, the SSL impedance

can be deduced as [34]

$$R_{SSL} = \sum_i \frac{(a_{c1i})^2}{C_{1i} f_{sw}} = \frac{2.88}{C_{eq} f_{sw}} \quad (6)$$

where C_{1i} represents the capacitance of capacitor $1i$. C_{eq} represents the uniform capacitance of each capacitor. f_{sw} represents the switching frequency. It can be seen that the SSL impedance directly represents the capacitor losses due to the charging and discharging of capacitors, which is inversely proportional to the switching frequency f_{sw} .

At high switching frequencies, the FSL impedance is dominated by the resistances of switches and interconnect. As shown in Fig. 3(a) and (b), the charges flowing through the switches during phases A and B can be given by

$$\begin{aligned} \mathbf{a}_r &= [a_{r11}^A \ a_{r12}^B \ a_{r13}^A \ a_{r14}^B \ a_{r15}^A \ a_{r16}^B \ a_{r17}^A \ a_{r18}^B]^T \\ &= \begin{bmatrix} \frac{6}{8} & \frac{6}{8} & \frac{2}{8} & \frac{2}{8} & -\frac{2}{8} & -\frac{2}{8} & -\frac{6}{8} & -\frac{6}{8} \end{bmatrix}^T \end{aligned} \quad (7)$$

where a_{r1i} represents the charge flowing through the switch during the single switching phase when the switch is ON. The total loss of the proposed equalizer at higher frequencies is the sum of the switch losses [34]. Thus, the FSL resistance can be given by

$$R_{FSL} = \sum_i \frac{R_{1i} (a_{r1i})^2}{D_{1i}} \quad (8)$$

where R_{1i} is the resistance of switch $1i$. D_{1i} is the duty cycle for switch $1i$.

At $D_{1i} = 50\%$, the FSL impedance can be derived as follows:

$$R_{FSL} = 2 \sum_i R_{1i} (a_{r1i})^2 = 5R_{eq} \quad (9)$$

where R_{eq} is the equivalent resistance of each switch, including the ON-state resistance and the interconnect resistance. It can be seen that the FSL impedance mainly represents the resistive conduction loss, which is independent of the switching frequency.

From (6) and (9), it can be concluded that the impedance of the proposed equalizer mainly depends on the charges flowing through the capacitors and switches.

Analogously, the SSL and FSL impedances of the CSCE [9], DTSCE [10], and SSSCE [31] can be derived. In order to achieve a fair comparison, it is assumed that each equalizer has the same total capacitance of capacitors, i.e., $C_{total} = 79.2 \mu\text{F}$. As a consequence, the capacitance of one capacitor of the CSCE [9], DTSCE [10], SSSCE [31], and proposed solution is 26.4, 19.8, 19.8, and 13.2 μF , respectively. Fig. 4 shows the impedance comparison of the proposed equalizer with the traditional SC methods versus the switching frequency at $R_{eq} = 0.3 \Omega$. It can be observed that the CSCE [9] has the largest SSL impedance because it can only transfer energy between two adjacent cells. The impedance of the DTSCE [10] is reduced significantly by introducing the second-tiered capacitor. The capacitors of the SSSCE [31] are connected in star, leading to a further decrease in impedance. By comparison, the proposed equalizer has the

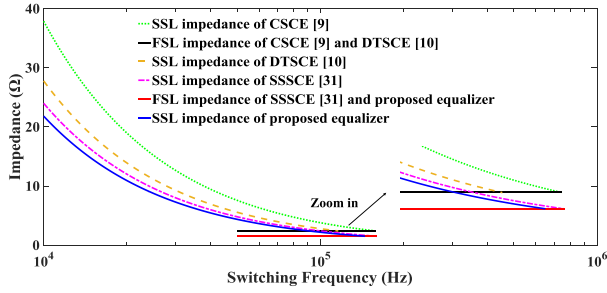


Fig. 4. Switching impedances of the proposed equalizer and the traditional SC methods versus the switching frequency.

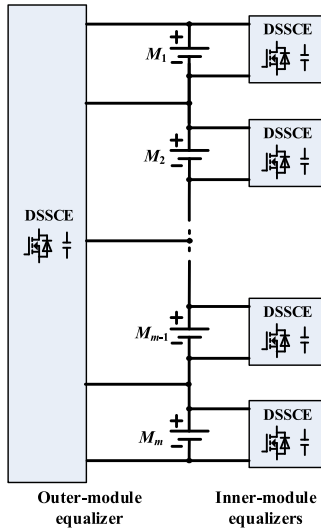


Fig. 5. Modularized structure of the proposed equalizer.

smallest impedance because of the delta-structured capacitors, resulting in a larger balancing current and a higher balancing efficiency. Moreover, the proposed equalizer has a smaller FSL impedance than the CSCE [9] and DTSCE [10]. It can be noted that the SSL impedance of the proposed equalizer will intersect with the FSL impedance at the frequency of 145 kHz, where the theoretical smallest impedance is achieved. However, the real switching frequency should be lower than the theoretical value due to the influence of the stray inductances.

D. Modularization Method of the Proposed DSSCE

Fig. 5 shows the modularized structure of the proposed equalizer, which includes m battery modules and n cells in each module. In this configuration, m inner module equalizers are set for m battery modules, to achieve the cell balancing of each battery module. In addition, due to each battery module regarded as a high-voltage battery cell, another outer module equalizer is set for the whole battery pack to achieve the balancing among battery modules. Therefore, the global AC2AC equalization for a multimodule battery string can be easily achieved by this module-based architecture. Although the maximum voltage stress on very few capacitors in the outer module equalizer is equal to the overall voltage of the battery pack, the voltage stress on the most capacitors in the inner module equalizers can be reduced dramatically. In summary, by modularizing a long

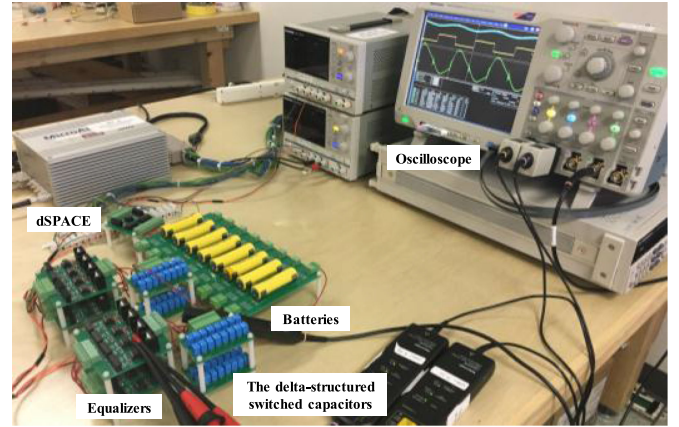


Fig. 6. Experiment setup for four LiFePO₄ cells.

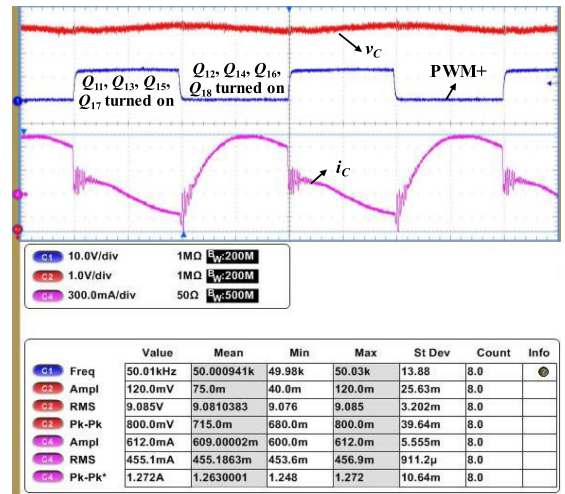


Fig. 7. Experimental waveforms at the switching frequency of $f = 50$ kHz.

battery string into a small number of battery modules, it can ensure that the design for a long battery string is more easy and flexible with a lower voltage stress on components, leading to a higher reliability.

III. EXPERIMENTAL RESULTS

Fig. 6 shows a photograph of the proposed DSSCE applied to eight 1100-mAh LiFePO₄ cells. To constitute the DSSCs, 13.2 μ F/10.6 m Ω film capacitors are implemented. A dSPACE was used for the digital controller. The balancing efficiency was calculated based on the total input and output powers of cells, which were measured by the YOKOGAWA WT1800 Precision Power Analyzer.

Fig. 7 shows the experimental waveforms of the proposed DSSCE at the switching frequency of $f = 50$ kHz, which agree with the theoretical analyses. Table I further presents the SSL impedances and measured rms currents of the proposed equalizer at different frequencies. It can be seen that at a lower switching frequency, e.g., 10 kHz, the balancing current is smaller due to the larger SSL impedance, i.e., 21.8 Ω . At a higher switching frequency, e.g., 100 kHz, the equivalent impedance is decided by the stray inductance in the circuit [35], also resulting in a

TABLE I
SWITCHING IMPEDANCES AND MEASURED RMS CURRENTS OF THE PROPOSED
EQUALIZER AT DIFFERENT SWITCHING FREQUENCIES

Switching frequency	10 k	25 k	50 k	100 k
SSL Impedance	21.8 Ω	8.7 Ω	4.4 Ω	2.2 Ω
RMS current	309.9 mA	441.3 mA	455.1 mA	304.0 mA

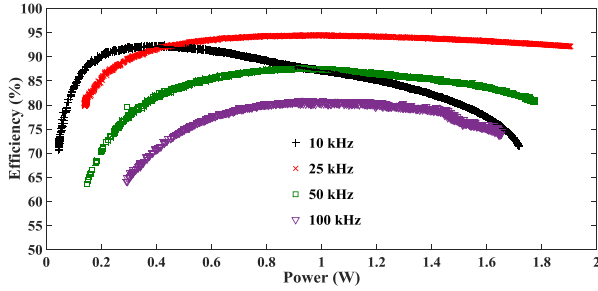


Fig. 8. Measured balancing efficiency η as a function of power at different frequencies.

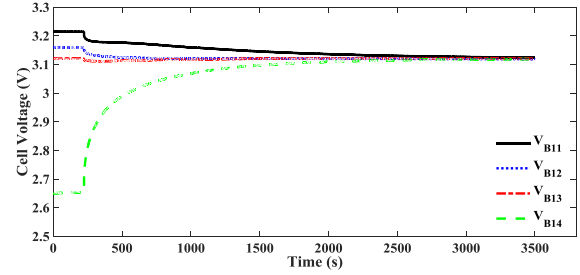
smaller balancing current, i.e., 304.0 mA. By comparison, the smaller SSL impedances, i.e., 4.4–8.7 Ω and larger balancing currents, i.e., 441–455 mA are achieved between 25 and 50 kHz.

Fig. 8 shows the measured efficiency η at different frequencies. It can be observed that due to the lower equivalent impedance, the proposed equalizer has higher efficiencies at 25 kHz. Moreover, the balancing efficiency curve becomes much flatter, which is over 90% at the output power changing from 0.31–1.90 W. Particularly, the peak efficiency is obtained as 94.5% when the output power is 0.91 W. Nevertheless, as the switching frequency decreases to 10 kHz or increases to 100 kHz, the balancing efficiency decreases significantly due to the larger equivalent impedance. This agrees well with the above-mentioned switching limit impedance analysis.

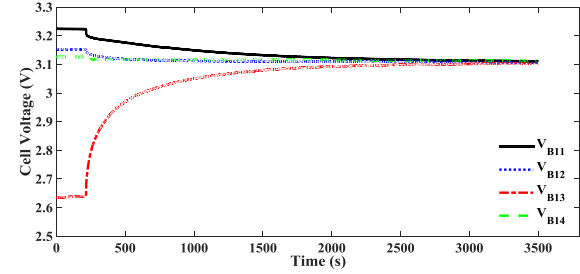
Fig. 9 presents the balancing results for four LiFePO₄ cells with different cell voltage distributions at $f = 25$ kHz. The initial cell voltages are 3.215, 3.160, 3.120, and 2.653 V. It can be observed that the proposed equalizer achieves a steady balancing performance with the same balancing time, i.e., 3500 s, almost the same balanced voltage, i.e., about 3.112 V, and almost the same voltage gap, i.e., about 7 mV, regardless of the imbalanced cases of the series-connected battery string.

Fig. 10 shows the experimental results for four LiFePO₄ cells at 10 and 100 kHz. The cells have the same initial cell voltages, as shown in Fig. 9(a). It can be observed that the balancing times become longer and the balanced voltages become lower due to the larger switching impedances at too low or high switching frequencies.

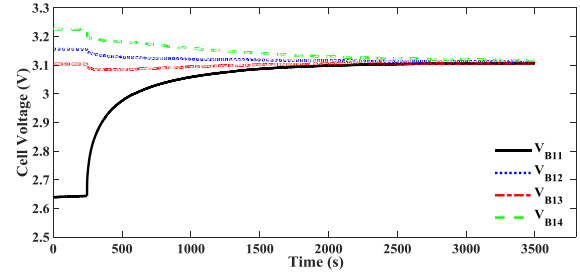
Fig. 11 shows the dynamic balancing results during battery constant-current charging and discharging. It can be seen that the proposed equalizer can ensure all the cells almost identically charged or discharged even though the battery string has a large initial voltage gap among cells. The consistency of the battery string during charging or discharging is greatly improved, showing a good dynamic balancing performance. It can be con-



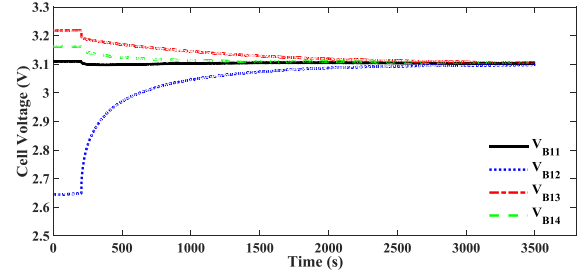
(a)



(b)



(c)



(d)

Fig. 9. Experimental results for four LiFePO₄ cells at $f = 25$ kHz. (a)–(d) With different cell voltage distributions.

cluded that the proposed equalizer has strong robustness and can be applied to any battery working state, e.g., rest, charging, or discharging.

Fig. 12 shows the comparative experimental results with the CSCE [9] and SSSCE [31], which have the same initial cell voltages, as shown in Fig. 9(a). As shown in Fig. 12(a), the CSCE [9] only transfers energy from one cell to the adjacent cell(s), leading to a longer balancing time, i.e., 20 000 s and a lower balanced voltage of 3.082 V. As shown in Fig. 12(b), the SSSCE [31] can simultaneously balance all the cell voltages to the average value. The total balancing time is reduced to 5000 s with the balanced voltage of 3.089 V. Compared with the balancing result shown in Fig. 9(a), it can be concluded that the proposed method has the clear advantages over the conventional SC ones in the balancing speed and efficiency.

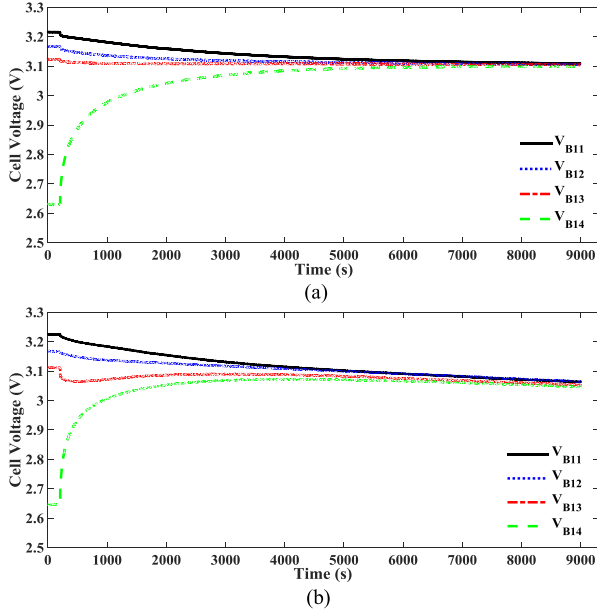


Fig. 10. Experimental results for four LiFePO₄ cells at different switching frequencies. (a) At $f = 10$ kHz. (b) At $f = 100$ kHz.

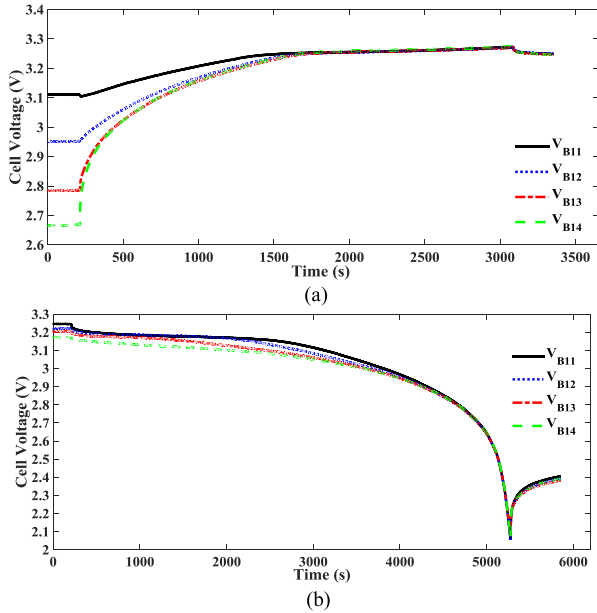


Fig. 11. Dynamic balancing results for four LiFePO₄ cells. (a) Battery charging. (b) Battery discharging.

IV. COMPARISON WITH CONVENTIONAL BATTERY EQUALIZERS

In order to identify the benefits of the proposed scheme, Tables II and III present a comparison of the proposed equalizer with the traditional solutions in terms of the components and the balancing performances, respectively. It is assumed that the battery string has 96 cells connected in series with 12 battery modules and 8 cells in one battery module. The component numbers and balancing performances of all the equalizers are calculated and evaluated based on the modularization method shown in Fig. 5.

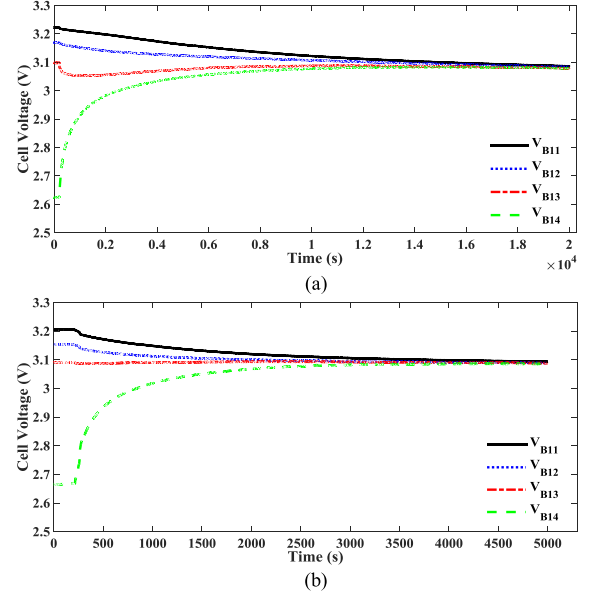


Fig. 12. Experimental results for four LiFePO₄ cells with the conventional SC methods. (a) CSCE [9]. (b) SSSCE [31].

In order to make a fair comparison, the size and cost of the equalizers are evaluated at the same balancing power. Therefore, the circuit size and cost mainly depend on the number of components, including MOSFETs (M), resistors (R), inductors (L), capacitors (C), diodes (D), and transformers (T). Particularly, a quantitative cost comparison can be achieved by calculating the total price of each equalizer [21]. In Table III, seven indexes are employed to evaluate the balancing performances, which are the balancing efficiency, current, mode, control strategy, switch stress, capacitor stress, and reliability. Mode is evaluated according to the balancing paths, i.e., AC2C, DC2C, P2C, C2P, and AC2AC. Control strategy is evaluated according to voltage-based, SoC-based, and automatic balancing methods. The reliability is approximately evaluated according to the number of components and the voltage stress on components, which is scored by “excellent (E),” “very good (VG),” “good (G),” “satisfactory (S),” and “poor (P).”

Compared with the SC-based equalizers, the CSCE [9] has the obvious advantages of smaller size, lower cost, lower voltage stress on capacitors and switches, i.e., 3.2 V. However, the biggest problem is that energy is only transferred between two adjacent cells, leading to a higher SSL impedance and smaller balancing current, i.e., 0.13 A.

The DTSCE [10] and the chain structure of SC equalizer (CSSCE) [11] employ an additional capacitor to achieve the opportunity to exchange charge directly between the top cell and the bottom one, resulting in a significant reduction in the SSL impedance and an increased balancing current, i.e., 0.25 A. In addition, the CSSCE [11] has a higher voltage stress on the additional switches, i.e., 304 V, while the DTSCE [10] withstands a higher voltage stress on the added capacitor, i.e., 304 V, leading to a lower reliability.

The series-parallel structure of SC equalizer (SPSSCE) [30] and the SSSCE [31] realize the automatic AC2AC balancing

TABLE II
COMPARISON OF THE PROPOSED EQUALIZER WITH THE TRADITIONAL SOLUTIONS IN TERMS OF COMPONENTS

Balancing methods	Components						Size	Cost (\$)①	
	SW	R	L	C	D	T			
CSCE [9]	216	0	0	95	0	0	Very small	775	Low
DTSCE [10]	216	0	0	108	0	0	Very small	777.6	Low
CSSCE [11]	268	0	0	121	0	0	Small	962.2	High
SPSSCE [30]	432	0	0	108	0	0	Large	1533.6	Very high
SSSCE [31]	216	0	0	216	0	0	Small	799.2	Low
Dissipative equalizer [8]	96	96	0	0	0	0	Very small	345.6	Very low
ZCS SC equalizer [12]	216	0	95	95	0	0	Large	851	Low
Buck-boost converter [14]	380	0	190	0	0	0	Very large	1482	Very high
Distributed equalizer [26]	768	0	0	0	0	96	Small	1536	Very high
Flyback converter [21]	190	0	0	0	190	13	Very large	1115	High
Forward/flyback converter [19]	216	0	0	0	0	13	Very large	1016	High
Forward converter [29]	108	0	0	108	0	13	Large	659.6	Very low
Proposed equalizer	216	0	0	402	0	0	Small	836.4	Low

① Component cost per unit (\$): MOSFET (2), MOSFET Driver IC (1.5), Resistor (0.1), Diode (1), Inductor (0.8), Capacitor (0.2), and Multi-Winding Transformer (20) [21].

TABLE III
COMPARISON OF THE PROPOSED EQUALIZER WITH THE TRADITIONAL SOLUTIONS IN TERMS OF BALANCING PERFORMANCES

Topologies	Efficiency	Current	Mode	Control strategy	Switch stress①	Capacitor stress①	Reliability
CSCE [9]	92.9%	0.13 A	AC2C	Automatic	3.2 V	3.2 V	E
DTSCE [10]	94.7%	0.25 A	AC2C	Automatic	3.2 V	304 V	E
CSSCE [11]	94.7%	0.25 A	AC2C	Automatic	304 V	3.2 V	P
SPSSCE [30]	95.3%	0.29 A	AC2AC	Automatic	152 V	3.2 V	P
SSSCE [31]	92.7%	0.29 A	AC2AC	Automatic	3.2 V	152 V	S
Dissipative equalizer [8]	0%	0.1 A	C2R	Voltage-based	3.2 V	-	E
ZCS SC equalizer [12]	94.1%	0.11 A	AC2C	Automatic	3.2 V	-	S
Buck-boost converter [14]	85.7%	0.25 A	AC2C	Automatic	3.2 V	-	S
Distributed equalizer [26]	$\eta^{2②}$	10 A	AC2AC	SOC-based	16 V	-	VG
Flyback converter [21]	88%	0.15 A	C2P	Voltage-based	304 V	-	P
Forward/flyback converter [19]	80.7%	2 A	DC2C	Voltage-based	3.2 V	-	VG
Forward converter [32]	93%	0.5 A	AC2AC	Automatic	3.2 V	-	P
Proposed equalizer	94.5%	0.46 A	AC2AC	Automatic	3.2 V	304 V	VG

① It is assumed that a cell voltage is 3.2 V.

② η represents the balancing efficiency of the distributed equalizer [26], whose measured value is unavailable.

under any imbalance circumstance, leading to a smaller SSL impedance and a larger balancing current, i.e., 0.29 A. However, the SPSSCE [30] has the main disadvantages of a higher cost and poor reliability due to the need of a larger number of switches and a higher voltage stress on switches, i.e., 152 V. The SSSCE [31] has a lower voltage stress on switches, i.e., 3.2 V, but has a higher voltage stress, i.e., 152 V on capacitors. Particularly, the energy must travel through two capacitors before arriving at the target cells, leading to a decreased balancing efficiency.

In summary, the existing SC-based solutions have the clear advantages of automatic, simultaneous and accurate balancing, and ease of implementation, but also have some limitations. For example, the CSCE and DTSCE have a lower balancing speed and efficiency dependent on the initial imbalanced cases of the cell voltages. The CSSCE and SPSSCE need more MOSFETs with a higher voltage stress, resulting in a lower reliability.

Compared with the non-SC equalizers, the dissipative equalizer [8] is the one being widely used in EVs, which has the advantages of small size and low cost. However, the energy is consumed instead of being transferred to the lower energy cells, so the balancing efficiency is 0.

A zero current switching (ZCS) SC equalizer [12] uses a capacitor and an inductor for every two adjacent cells, which is heavier and larger compared with the CSCE [9]. As the name implies, the main advantage of this method is the zero switching loss and the low switch current stress. However, due to the AC2C equalization, the balancing efficiency and speed would become lower as the cell number increases.

The buck-boost converter [14] can achieve the automatic and simultaneous balancing between every two adjacent cells with a simple control. The main advantage is the modularization design and low voltage stress on switches. However, this method needs

a large number of switches and inductors, leading to a larger size and higher cost.

The distributed equalizer [26] can realize the AC2AC equalization with a 10-A balancing current for one cell. Therefore, this method has the fastest balancing speed. It is worth mentioning that this approach can realize the SoC-based balancing for the battery string, which maximizes the available capacity of the battery string. Another advantage is its modularity, allowing easy system extension to a larger number of cells. However, one dc-dc bypass converter is needed for each cell, leading to a higher cost. Moreover, the balancing energy must travel through two bypass converters from the source cell to the target one, leading to a reduced balancing efficiency.

The time-shared flyback converter [21] can achieve the C2P equalization using a single transformer. Nonetheless, this topology requires a large quantity of MOSFET switches as well as diodes and needs voltage-monitoring circuits to decide which cell has the highest voltage, resulting in a larger size, higher cost, and more complex control. Moreover, the balancing speed is lower due to the time-shared equalization for cells.

The forward conversion method [29] only needs one MOSFET for one cell, leading to a lower cost, and can realize automatic and simultaneous voltage equalization among cells without the requirement of cell monitoring circuits, resulting in a higher balancing speed and efficiency. However, this solution requires a multiwinding transformer for a battery string, leading to the mismatching of multiple windings and bulk size. Thus, the main disadvantages are the low reliability and poor balancing effect.

Compared with the existing equalizers, the proposed solution is an improvement of the conventional SC methods, which achieves the automatic AC2AC balancing with a larger balancing current, i.e., 0.46 A and higher balancing efficiency, i.e., 94.5% without significant changes compared with the conventional SC equalizers. The proposed equalizer has also some advantages over the non-SC topologies, e.g., the higher balancing efficiency, ease of control, automatic AC2AC equalization, high-accuracy equalization, etc. However, the disadvantages are that the proposed solution needs more capacitors with higher voltage stress.

V. CONCLUSION

The objective of this paper is to introduce a cost-effective balancing topology without significant increases in hardware and control compared with the classical SC equalizer so that it can meet the application requirements of EVs for performance, reliability, size, and cost. A DSSCE was proposed and a prototype for four cells was tested. The configuration of the proposed equalizer, operation principles, SSL and SFL impedance analysis, balancing performances, and comparison with the conventional methods were presented. The limit impedance analysis showed the proposed equalizer had smaller SSL impedance than the conventional SC methods, leading to a higher balancing efficiency and speed. Experimental results demonstrated that the proposed system achieved the fast AC2AC equalization, which was independent of the cell number and the initial imbalanced statuses of battery strings.

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Yunlong Shang (S'14–M'18) received the B.S. degree in automation from Hefei University of Technology, Hefei, China, in 2008, and the Ph.D. degree in control theory and control engineering from Shandong University, Jinan, in 2017.

Between September 2015 and October 2017, he conducted scientific research as a joint Ph.D. student at the Department of Energy funded Graduate Automotive Technology Education Center for Electric Drive Transportation, San Diego State University, San Diego, CA, USA, where since 2017, he has been

a Postdoctoral Research Fellow. His current research interests include battery equalizers, battery modeling, battery states estimation, and battery management systems of electric vehicles.



Chenghui Zhang (M'14–SM'17) received the Bachelor's and Master's degrees in automation engineering from Shandong University of Technology, Jinan, China, and the Ph.D. degree in control theory and operational research from Shandong University, Jinan, in 1985, 1988, and 2001, respectively.

In 1988, he joined Shandong University, where he is currently a Professor with the School of Control Science and Engineering, the Chief Manager of Power Electronic Energy-Saving Technology and Equipment Research Center of Education Ministry, a

Specially Invited Cheung Kong Scholars Professor by China Ministry of Education, and a Taishan Scholar Special Adjunct Professor. He is also one of the state-level candidates of "The New Century National Hundred, Thousand and Ten Thousand Talent Project," the Academic Leader of Innovation Team of Ministry of Education, and the Chief Expert of the National "863" high technological planning. His research interests include optimal control of engineering, power electronics and motor drives, energy-saving techniques, and time-delay systems.



Naxin Cui (M'14) received the B.S. degree in automation from Tianjin University, Tianjin, China, in 1989, and the M.S. and Ph.D. degrees in control theory and applications from Shandong University, Jinan, China, in 1994 and 2005, respectively.

In 1994, she joined Shandong University, where she is currently a Full Professor with the School of Control Science and Engineering. Between December 2016 and February 2017, she conducted scientific research as a Visiting Scholar with the Department of Energy funded Graduate Automotive Technology Education Center for Electric Drive Transportation, San Diego State University, San Diego, CA, USA. Her current research interests include power electronics, motor drives, automatic control theory and application, and battery energy

management system of electric vehicles.



Chunting Chris Mi (S'00–A'01–M'01–SM'03–F'12) received the B.S.E.E. and M.S.E.E. degrees from Northwestern Polytechnical University, Xi'an, China, in 1985 and 1988, respectively, and the Ph.D. degree from the University of Toronto, Toronto, ON, Canada in 2001, all in electrical engineering.

He is a Professor and the Chair of electrical and computer engineering and the Director of the Department of Energy funded Graduate Automotive Technology Education Center for Electric Drive Transportation, San Diego State University (SDSU), San

Diego, CA, USA. Prior to joining SDSU, he was with the University of Michigan, Dearborn, from 2001 to 2015. His research interests include electric drives, power electronics, electric machines, renewable-energy systems, and electric and hybrid vehicles.